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A High-Efficiency DC-DC Converter Based on Series/Parallel Switched Inductor Capacitors for Ultra-High Voltage Gains

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Abstract: A high-efficiency DC-DC converter employing a modified architecture called the hybrid switched inductor–capacitor series (MHSLCS) is proposed in this paper. The primary goal is to achieve a notably ultra-high voltage gain for renewable energy systems (RESs). Furthermore, the use of only one input capacitor in the MHSLCS eliminates pulsations in the input current at both low and high duty ratios. The proposed converter integrates the MHSLCS with a modified switched capacitor (MSC) that interleaves with the main MOSFET, effectively doubling the voltage transfer gain. Additionally, a modified hybrid switched inductor–capacitor parallel (MHSLCP) is incorporated in parallel with an interleaved auxiliary MOSFET. Both MOSFETs, combined with the MSC, contribute to achieving an ultra-high voltage gain. In addition, the inductors of the MHSLCP operate in a discontinuous conduction mode (DCM), which results in significant stress reductions in the power diodes and switches at high output voltages. The advantages of the proposed converter are multifaceted, demonstrating a high efficiency while minimizing the voltage in power device diodes and MOSFETs. The use of low inductance and capacitance values at high switching frequencies further enhances the performance. Wide-bandgap (WBG) power devices are employed to achieve the desired high voltage gain and efficiency. The proposed converter was designed with a PCB and underwent experimental testing to validate laboratory results. The proposed converter boosted the input voltage from 30 V to a variable output voltage between 325 V and 500 V, with a power output of 325 watts and an efficiency of 95.5%.

Keywords: MHSLCS; MHSLCP; switched capacitor; switched converter; high-efficiency DC-DC converter

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1. Introduction

The growing interest in harnessing renewable energy sources (RESs) for electricity generation reflects a global commitment to energy security and environmental sustainability [1,2]. While solar energy has seen widespread adoption, the inherent challenge of the variable low-voltage output of photovoltaic panels hinders their applicability for high DC supply voltage needs. Addressing this limitation, the integration of DC-DC converters becomes imperative, facilitating voltage boosts for diverse applications, including LED streetlights, medical equipment, uninterruptible power supplies, and microgrid systems [3,4]. Researchers have explored various DC–DC conversion techniques to achieve high voltage gains, such as SEPIC and boost converters. However, these face challenges like reduced component counts, efficiency issues at high voltage gains, and increased stress on power switches [1,5]. Consequently, numerous researchers have proposed different technologies for DC-DC converters, which can be broadly categorized into two types: isolated converters that utilize coupled inductors or transformers, and non-isolated converters that employ coupled inductors without transformers. A modified DC-DC boost converter was introduced with a coupled inductor for enhanced performance in [1]. For isolation needs, in [6], a full bridge with an isolation transformer interleaved flyback DC-DC converter

is suggested. Additionally, a boost-SEPIC DC-DC converter integrating soft switching techniques for voltage regulation in PV systems is presented in [7]. Similarly, a non-isolated DC-DC converter based on the diode–capacitor technique utilizing a coupled inductor is introduced in [8–10]. Likewise, a non-isolated DC-DC converter employing an interleaved structure with coupled inductors and a switched capacitor, resulting in an improved voltage conversion ratio, is proposed in [9–24]. These converters have exhibited notable achievements in terms of high voltage gains.

However, they are plagued by certain limitations that impede their overall performance. These drawbacks include the excessive utilization of both passive and active elements, a substantial count of diodes, an increase in the parasitic resistance of inductors and capacitors, and a consequent reduction in efficiency. Furthermore, the pursuit of achieving a high voltage gain by augmenting the turn ratio of coupled inductors results in an escalation in internal resistance, further compromising the system's efficiency [5,11–35]. An additional challenge arises from the low switching frequency employed by these converters, necessitating the use of bulky inductors and capacitors. Furthermore, the voltage gain is adversely affected by the on-resistance (Ron) of the power MOSFET, which decreases the efficiency of the system. Moreover, the presence of coupled inductor converters generates high spike voltages during the off state of the power switch due to the inductance of the parasitic capacitance associated with the power MOSFET switch. To tackle this issue, a clamped circuit may be introduced in the power switch [6–10].

Researchers have explored innovative approaches to enhance voltage gains in DC-DC converters. In [12–34], a modified DC-DC converter based on interleaved boost and buck-boost topologies is presented, integrating extendable switched capacitor cells for stand-alone PV systems. In [13,14], a modified SEPIC-based step-up converter combining a quasi-Z-source (qZS) and a switched capacitor network was presented for improved performance. In [15–21], a hybrid switched inductor and a switched-capacitor-based quasi-Z-source DC-DC boost converter were introduced, leveraging the strengths of both for efficient voltage conversion. For non-isolated high gain converters, in [17–26], a design integrating a dual boost converter with a switched inductor structure was proposed to reach high conversion ratios. In [19–28], a comprehensive DC-DC converter is presented, combining a switched inductor, a switched capacitor, and voltage multiplier stages with a traditional boost converter to enhance voltage conversion capabilities. Moreover, in [14], a hybrid non-isolating cluster switched inductor boost with a hybrid DC-DC converter is introduced, aiming to achieve remarkable voltage gains.

These advancements showcase diverse strategies for achieving superior voltage performance in DC-DC conversion. Conversely, other researchers have explored alternative approaches, resulting in the development of non-isolation DC-DC converters capable of achieving high voltage gains without relying on transformers and coupled inductors. These converters are based on the switched inductor and switched capacitor techniques. For electric vehicles (EVs) and solar PV installations, a bidirectional DC-DC converter based on a switched inductor is presented in [9], combining MOSFET switches and bidirectional switches to achieve a high voltage gain. Building upon this concept, refs. [16–22] propose a bidirectional hybrid DC-DC converter that combines a switched capacitor and a switched inductor, resulting in higher voltage conversion ratios. In [23–25], a high voltage gain boost converter is proposed that incorporates switched inductor and switched capacitor techniques in conjunction with a modified voltage multiplier cell and a double voltage multiplier cell configuration, which was first introduced in [31]. Despite their remarkable capacity to verify substantial voltage gain, these previous converters exhibit limitations. The elevated voltage gain necessitates an excessively high duty cycle, resulting in amplified MOSFET conduction and switching losses and diminished efficiency [1–35]. Additionally, the heightened duty cycle places substantial voltage strain on essential components such as power switches, diodes, and inductors, potentially affecting their longevity. Furthermore, these converters operate at a low switching frequency, often integrating numerous induc-

tors [5,36]. This inadvertently introduces elevated levels of parasitic resistance, limiting their effectiveness in practical applications.

Further modifications are proposed. In [3,4], a non-isolated extendable DC-DC converter is presented, employing (APIC) active–passive inductor cells to optimize voltage conversion. Moving converter topologies in [11] describe a switched capacitor with a large count of components offering step-up voltage. A DC-DC converter based on an (ANC) active-network converter with a switched capacitor technique is proposed in [15–31], emphasizing performance enhancements in RESs. In the pursuit of high-gain configurations, ref. [19] introduces a high-gain boost converter employing an extended single-switch high-gain topology, utilizing multi-cell configurations for RESs. Similarly, [20,33] presents a high-gain DC-DC converter based on a multi-cell hybrid switched-inductor (HLS) topology, specifically designed to achieve high voltage ratios. In [29], three types of converters are developed: the switched inductor-boost, SC-boost, and ANC converters, each offering voltage regulation. In [30], a novel switched-inductor double-switch DC-DC converter (SL-DS-DC) is introduced with a redesigned switched inductor arrangement, aiming to enhance efficiency in PV systems. In [17–27], improved hybrid switched inductor switched-capacitor DC-DC converters are introduced, with a high number of power switches. However, despite their ability to achieve high voltage gain ratios, these converters exhibit drawbacks that affect their performance and limit their usefulness, including the need for high duty ratios, increased losses, reduced efficiency at high voltage gain, and a negative impact on component durability [32].

This paper introduces a high-efficiency DC-DC converter utilizing the MHSLCS interleaved with an MSC and MHSLCP. The primary goal of this design is to validate exceptionally high voltage gain in photovoltaic applications. To achieve this objective, the proposed converter incorporates an MHSLCS with an MSC interleaved with the main switch, effectively doubling the voltage transfer gain. Additionally, the MHSLCP, serving as interleaved components, is integrated in parallel into the converter design with an auxiliary switch. This design not only optimizes voltage transfer gain but also ensures low voltage stress across the auxiliary switch by combining the main switch and auxiliary switch with the MSC. Furthermore, each pair of inductors is connected in series, with both having the same voltage and current, aiming to reduce the number of passive elements and enhance the overall performance of the proposed converter. In addition, the series–parallel inductors have very low voltage across them when the converter supplies 500 V output voltage. In addition, the inductors of the MHSLCP operate in DCM, which leads to significant stress reduction in power diodes and switches at high output voltage. In addition, the proposed converter operates at high efficiency when the inductors of the MHSLCP operate in DCM. This means that the voltage stress across power switches and diodes is significantly reduced when the proposed converter operates at high power applications. In addition, the inclusion of only one input capacitor serves to eliminate pulsations in input current at both low and high duty ratios. Additionally, a dual PI controller is designed as the control strategy for the proposed converter. This controller is designed to validate constant output voltage while accommodating variable input voltage, contributing to the robust performance of the system.

2. Structure and Operation Principle of the Proposed Converter

An ultra-high-gain DC-DC converter was used to verify high efficiency and load power applications for RESs, facilitating the elevation of low input voltages ranging from 25 V to 40 V to variable output voltages of 325 V to 500 V, while accommodating a 325 W load. In Figure 1a, the integrated setup of the proposed converter with PV Panels and applications, inverter, and load is depicted. The schematic diagram of the proposed converter is illustrated in Figure 1b. Comprising four primary inductors, five capacitors, seven diodes, and two MOSFETs, as shown in Figure 2a, the proposed converter boasts a simplified structure with numerous advantages. Sw_1 is the main first switch and Sw_2 is the auxiliary MOSFET. One notable advantage is the elimination of the need for coupled inductors and

transformers traditionally required for voltage step-up. The reduction in the values of capacitors and inductors, after the proposed converter operates at a high switching frequency, is significantly high, thereby enhancing overall efficiency. The converter's structure is simple to implement. The addition of a single input capacitor eliminates pulsations in the input current, even at very low duty cycles, enhancing its reliability—especially for photovoltaic applications. Moreover, the diodes in the MHSLCS, namely D_1 and D_2, experience remarkably low voltage stress. Furthermore, the proposed converter ensures low voltage stress on both the main and auxiliary switches. This feature enhances the reliability and longevity of the switches, minimizing the risk of failure and improving overall performance. By effectively managing voltage stress, the converter provides a more robust and durable solution for high voltage gain applications. The proposed converter achieves a higher voltage gain compared to previous DC-DC converters while employing fewer inductors and capacitors. The PWM generator controlling the MOSFET switches is simple, with both devices turning on and off simultaneously, simplifying the control mechanism.

2.1. Operation of the Proposed Converter

The proposed converter can operate in two different modes: the first one is referred to as DCM. This mode occurs when the converter operates at a low duty ratio and light load during the night in energy-saving mode. Additionally, the DCM mode is activated when the converter operates at the minimum input voltage in light load applications. Moreover, the proposed DC-DC converter can switch to continuous conduction mode (CCM) when the load current increases during the day.

2.2. Operation of the Proposed Converter in DCM

Mode 1: [0 to t0]. In this mode, both MOSFETs, Sw_1 and Sw_2, are turned on at the same time. The diodes D_1, D_2, D_5, and D_6 are in an on state while D_3, D_4, and D_7 remain off. L_1 starts charging energy from the input source, and L_2 charges energy from the input source through D_1; both inductors have the same current. C_1 releases energy through D_2 and Sw_1. Capacitors C_2 and C_3 store power and act as a dual source, which is used to charge L_3 through Sw_2. At the same time, L_4 charges from C_2 and C_3 through D_5; both inductors have the same current. C_4 releases energy through D_6, and C_5 supplies energy to the load. The proposed converter for this mode is shown in Figure 2b. The voltage and current equations for the different components during Mode 1 are as follows, where (Iin) is the input current.

$$\left.\begin{array}{l} V_{L_1} = Vg \\ V_{L_2} = Vg \\ V_{L_3} = Vc_2 + Vc_3 \\ V_{L_4} = Vc_4 \\ Vc_4 = Vc_2 + Vc_3 \\ Vc_5 = V_o \end{array}\right\} \quad (1)$$

$$\left.\begin{array}{l} Iin = iL_1 + iL_2 + Ic_1 \\ I_{SW1} = Iin + Ic_1 \\ I_{D1} = Iin - iL_1 \\ I_{D2} = Ic_1 + iL_2 \end{array}\right\} \quad (2)$$

$$\left.\begin{array}{l} Ic_4 = Ic_2 \\ I_{SW2} = Ic_3 = Ic_2 \\ I_{D6} = Ic_4, \\ I_{D5} = Ic_2 \\ Ic_5 = Io \end{array}\right\} \quad (3)$$

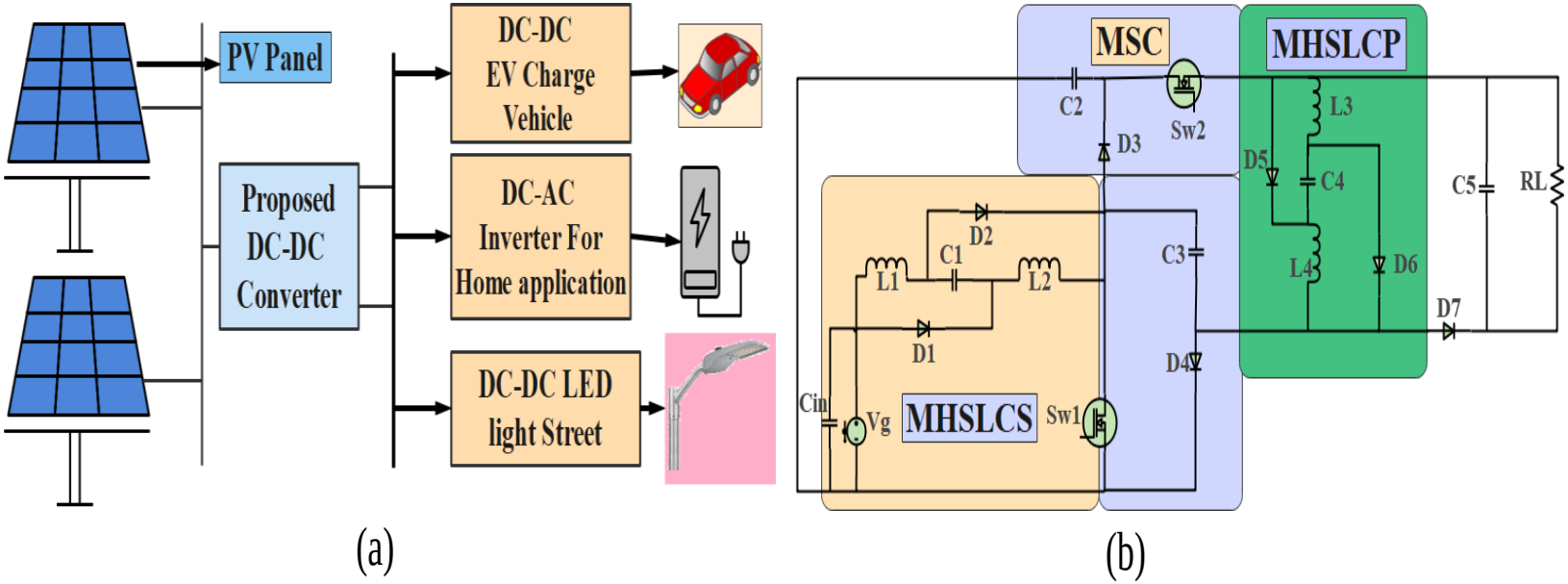


Figure 1. (**a**) The proposed converter integrated with PV Panels with applications. (**b**) The proposed DC–DC converter.

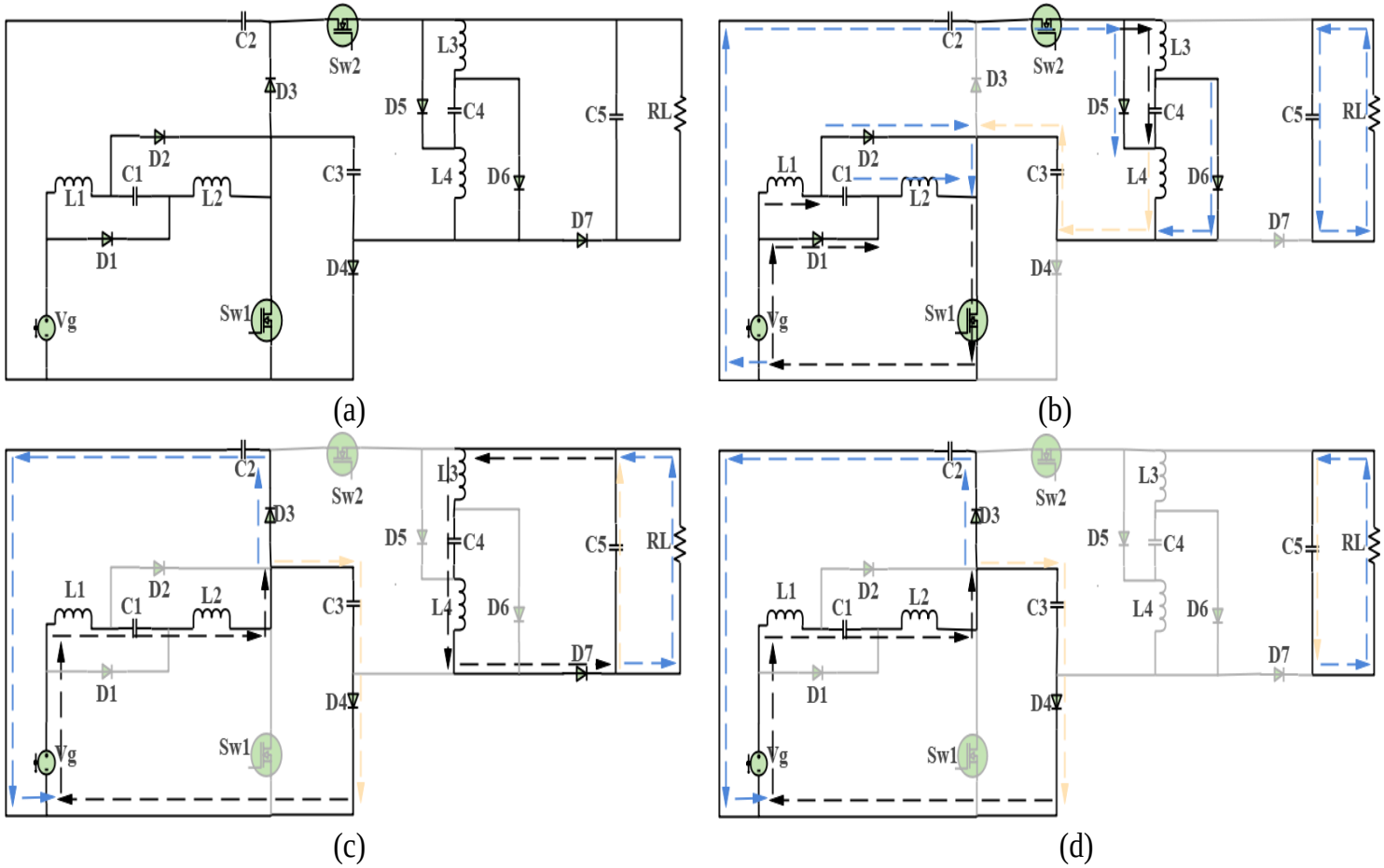


Figure 2. (**a**) The proposed DC–DC converter; (**b**) Mode 1 DCM, Mode 1 CCM; (**c**) Mode 2 DCM, Mode 2 CCM; (**d**) Mode 3 DCM.

Mode 2: [t0-t1]: During this mode, both MOSFETs are turned off, and certain diodes (D_1, D_2, D_5, and D_6) are also turned off. The inductor L_1 transfers its energy to capacitor C_1 through a series connection with L_2. At the same time, L_1 and L_2 discharge their energy to charge capacitors C_2 and C_3 through diodes D_3 and D_4. C_4 starts to accumulate energy from inductor L_3. In this mode, L_3 and L_4 are connected in series. Capacitor C_5 collects a significant amount of energy from L_3 and L_4 during the discharge period and provides high power to the load through diode D_7. The currents flowing through L_3 and L_4 are equal and become zero at (D1) simultaneously in this mode as shown in Figure 3a. The configuration for this mode is shown in Figure 2c. The voltage and current equations for the components in this state are as follows:

$$\left.\begin{array}{l} V_{L_1} + V_{L_2} = Vg + Vc_1 - Vc_2 \\ V_{L_3} + V_{L_4} = Vc_4 - V_o \\ Vc_5 = V_o \end{array}\right\} \quad (4)$$

$$\left.\begin{array}{l} V_{L_1} + V_{L_2} = 2Vg - Vc_1 - Vc_2 \\ V_{L_3} + V_{L_4} = Vc_4 - Vc_5 \\ Vc_5 = V_o \end{array}\right\} \quad (5)$$

$$\left.\begin{array}{l} Iin = iL_1 = iL2 = Ic_1 = I_{D3} = Ic_2 \\ Ic_4 = iL_3 = iL_4 \\ I_{D3} = I_{D4} = \frac{iL1}{2} \\ I_{D6} = iL_3 = iL_4 = Ic_5 \end{array}\right\} \quad (6)$$

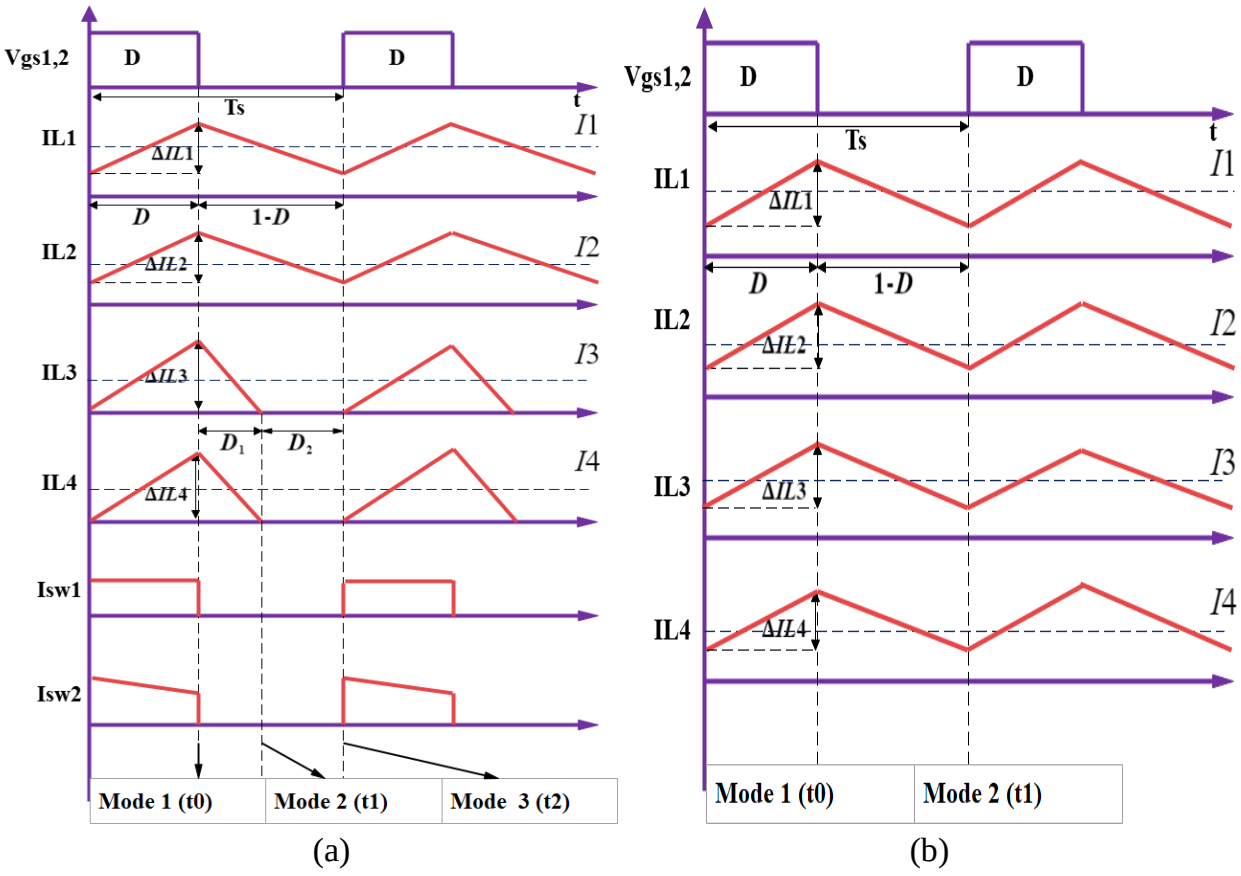


Figure 3. (**a**) Waveform of the proposed converter in DCM. (**b**) Waveform of the proposed converter in CCM.

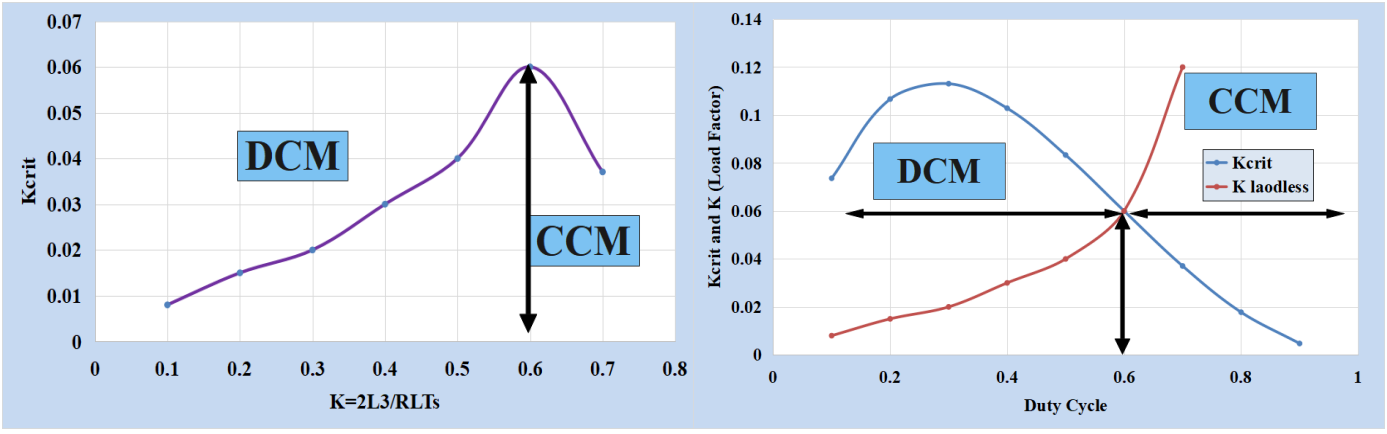
Mode 3: [t1-t2]: Both MOSFETs stay turned off, and diodes D_1, D_2, D_5, and D_6 also remain off. The energy stored in inductors L_1 and L_2 continues to discharge and charge capacitors C_2 and C_3. The energy in inductors L_3 and L_4 decreases to zero at time (D_2). Moreover, capacitor C_5 continues to provide power to the load. The configuration of the converter in this mode is shown in Figure 2d. The voltage and current equations remain unchanged from the previous mode. Figure 3a illustrates that inductor currents L_1 and L_2 operate in CCM, while L_3 and L_4 operate in DCM when the proposed converter operates in DCM mode. The current equation remains the same as in the previous mode.

2.3. Operation of the Proposed Converter in CCM

When the load current increases, the converter operates in CCM as depicted in Figure 3b. In CCM, both the input current and the current through all inductors are operating in CCM. Moreover, the voltage transfer ratio of the converter significantly increases in this mode. Figure 3b illustrates the two operation modes for this situation and shows the corresponding current waveforms of the proposed converter operating in CCM.

Mode 1: [0 to t0]: The MOSFETs Sw_1 and Sw_2 are both turned on simultaneously, resulting in the diodes D_1, D_2, D_5, and D_6 being switched on. Meanwhile, D_3, D_4, and D_7 are in the off state. L_1 starts linearly charging energy from the input source, and L_2 begins to charge energy from the input source through D_1. C_1 starts discharging energy through D_2 through Sw_1. During this mode, capacitors C_2 and C_3 act as a dual source, storing a significant amount of power that is used to charge L_3 through Sw_2, while L_4 starts charging from C_2 and C_3 through D_5. C_4 starts discharging energy through D_6. C_5 provides energy to the load. The proposed converter for this mode is illustrated in Figure 2b.

Mode 2: [t0-t1]: Both MOSFETs are turned off, while diodes D_1, D_2, D_5, and D_6 are in the off state. The inductor L_1 discharges its energy to capacitor C_1 through L_2. In this mode, L_1 and L_2 are connected in series. Meanwhile, L_1 and L_2 begin discharging their energy to charge capacitors C_2 and C_3 through D_3 and D_4. C_4 starts accumulating energy from L_3. In this mode, both L_3 and L_4 are in series. Capacitor C_5 accumulates a significant amount of energy from L_3 and L_4 during the discharging period and supplies high power to the load through D_7. The proposed converter for this mode is illustrated in Figure 2c. Figure 3b shows that all inductor currents are in CCM when the proposed converter operates in CCM mode, and the load current increases above 60% duty ratio, as shown in Figure 4a,b.



(a) (b)

Figure 4. The proposed converter dynamic performance: (**a**) K (Kcrit) vs. K load factor (**b**); Kcrit and K vs. duty cycle.

Figure 4a,b show the dynamic performance of the proposed converter in DCM and CCM. It can be seen that from the condition in Equation (25), the proposed converter can operate in DCM when the duty ratio is below 0.6 in CCM, the load current increases at the duty ratio above 60%, and the proposed converter supply is around 2 KW.

3. Voltage Transfer Gain Calculation

The voltage gain of the converter is calculated when the proposed converter operates in DCM and CCM to verify the gain performance and compare it with the previous converters.

3.1. Voltage Transfer Gain in CCM

The proposed converter can operate in CCM when the converter supplies a high load current. The volt-second balance equation in a DC-DC converter is a fundamental principle based on the conservation of energy for an inductor over a switching cycle. It is expressed as in Equation (7). This equation ensures that the total energy transferred during one switching cycle is conserved, balancing the volt-seconds on the input and output sides of the converter. Therefore, the voltage gain of the proposed converter is derived in CCM, as shown in the equations below.

$$\frac{1}{Ts}(\int_0^{Ts}(V)dt = 0 \tag{7}$$

$$\frac{1}{Ts}(\int_0^{DTs}(2Vg)dt + \int_D^{Ts}(Vs + Vc_1 - Vc_2)dt = 0 \tag{8}$$

$$\frac{1}{Ts}(\int_0^{DTs}(Vc_2 + Vc_3)dt + \int_0^{DTs}(Vc_4)dt + \int_D^{Ts}(Vc_2 + Vc_3 - V_o)dt = 0 \tag{9}$$

$$iL_1 = iL_2 = \frac{VgDTs}{L_2}(L_2 = L_1) \tag{10}$$

$$iL_3 = iL_4 = \frac{4VgDTs}{(1-D)L_3}(L_3 = L_4) \tag{11}$$

$$Vc_1 = Vg \tag{12}$$

$$Vc_2 = \frac{2Vg}{(1-D)} = Vc_3 \tag{13}$$

$$V_o = \frac{(D+1)(Vc_2 + Vc_3)}{(1-D)} \tag{14}$$

$$Mdc(CCM) = \frac{V_o}{Vg} = \frac{4(1+D)}{(1-D)^2} \tag{15}$$

Equations (1) and (4) form the foundation, with the application of volt-second balance to inductors L_1, L_2, L_3, and L_4 leading to the derivation of Equations (8) and (9). The solutions to these equations are presented in (13) and (14). The peak current of the inductors is expressed by Equations (10) and (11) for each of the four inductors. Equation (12) describes voltage across C_1, which is equivalent to the input voltage source. Equation (15) presents the voltage gain equation (Mdc) of the proposed converter in CCM. It is worth highlighting that, as evident from Equation (15), the proposed converter demonstrates superior voltage gain compared to previous converters.

3.2. Voltage Transfer Gain in DCM

$$\left.\begin{array}{l}\frac{1}{Ts}(\int_0^{DTs}(2Vg)dt + \int_D^{Ts}(Vs + Vc_1 - Vc_2)dt = 0\\ \frac{1}{Ts}(\int_0^{DTs}(Vc_2 + Vc_3)dt + \int_0^{DTs}(Vc_4)dt + \\ \int_D^{D1Ts}(Vc_4 - V_o)dt = 0\end{array}\right\} \tag{16}$$

$$\frac{Vc_2}{Vg} = \frac{2}{(1-D)} \tag{17}$$

$$D1 = \frac{4Vg(1+D)}{Vo(1-D)} \tag{18}$$

Equations (1) and (4) lay the groundwork, and applying the volt-second balance of Equation (7) to L_1, L_2, L_3, and L_4 leads to the derivation of Equation (16). Solving this equation produces the results presented in Equations (17) and (18). Notably, Equation (16) can be solved by leveraging the fact that the average Vc_1 equals Vg, as indicated in Equation (12). The parameter (D1), denoting the discharging time of L_3 and L_4, can be determined from Equation (18) after solving Equation (16). Equations (19) and (20) provide the average inductor current in L_3 and L_4, respectively.

$$< I3 >= \frac{2VgD(D+D1)}{fsL_3(1-D)} \tag{19}$$

$$< I4 >= \frac{2VgD(D+D1)}{fsL_3(1-D)} \tag{20}$$

$$I_o = \frac{(Vc_2+Vc_3)DD1}{2fsL_3} \tag{21}$$

$$Mdc(DCM) = \frac{8VgDRL(1+D)}{fsL_3V_o(1-D)^2} \tag{22}$$

$$Mdc(DCM) = \frac{4\sqrt{D(1+D)}}{(1-D)\sqrt{K}} \tag{23}$$

$$k_{crit} = \frac{D(1-D)^2}{(D+1)} \tag{24}$$

$$Kcrit = \begin{cases} if \text{ Kcrit} > \text{ (K) The Proposed Converter work in DCM} \\ if \text{ Kcrit} < \text{(K) The Proposed Converter work in CCM} \end{cases} \tag{25}$$

Equation (21) yields the average Io. Equation (22) represents the relationship between output voltage and input voltage source when the converter is operating in DCM. It is worth noting that, from Equation (22), it can be seen that voltage gain Mdc is contingent on (RL, D, Fs). The voltage gain of the proposed converter as a function of the load loss factor (K) can be found in Equation (23). The critical value of K (Kcrit) can be determined using Equation (23), leading to the formulation of Equation (24). The boundary condition between the DCM and CCM operation modes is defined by the condition in Equation (25).

4. Voltage Stress Calculations across Power MOSFETs, Diodes, and Capacitors

When designing a DC-DC converter, engineers perform voltage stress calculations for MOSFETs, diodes, and capacitors to determine the maximum voltage these components experience under various operating conditions. These calculations are essential for selecting components with sufficient voltage ratings, ensuring the converter's reliability and longevity.

Utilizing Equations (26) and (27), it becomes feasible to determine the voltage stress across D_1 and D_2. Notably, this voltage was found to be very small and dependent on the Vg over the period wherein the Vg ranged from 25 V to 40 V. Furthermore, Equations (28) and (29) contribute to the understanding of the voltage stress across D_3 and D_4.

$$V_{D_1} = \frac{Vg}{(1-D)} \tag{26}$$

$$V_{D_2} = \frac{Vg}{(1-D)} \tag{27}$$

$$V_{D_4} = \frac{2Vg}{(1-D)} \tag{28}$$

$$V_{D_3} = \frac{2Vg}{(1-D)} \tag{29}$$

$$V_{D_5} = \frac{4Vg}{(1-D)} \tag{30}$$

$$V_{D_6} = \frac{4Vg}{(1-D)} \tag{31}$$

$$V_{D_7} = Vo - \frac{4Vg}{(1-D)} \text{ as average value} \tag{32}$$

To further enrich the analysis, Equations (30)–(32) offer insights into the determination of VD_5, VD_6, and VD_7, providing a comprehensive view of the voltage distribution across various components within the proposed converter.

$$Vsw_1 = \frac{2Vg}{(1-D)} \tag{33}$$

$$Vsw_2 = \frac{6Vg}{(1-D)} \text{ as average value} \tag{34}$$

Leveraging Equations (33) and (34) facilitates the calculation of the voltage stress across Sw_1 and Sw_2, revealing that these values are very small when the proposed converter supplies a high load current.

$$Vc_1 = Vg \tag{35}$$

$$Vc_2 = \frac{2Vg}{(1-D)} \tag{36}$$

$$Vc_3 = \frac{2Vg}{(1-D)} \tag{37}$$

$$Vc_4 = \frac{4Vg}{(1-D)} \tag{38}$$

$$Vc_5 = V_o \tag{39}$$

Equation (35) succinctly represents the voltage across C_1, confirming its equality to the Vg. Moving forward, Equations (36) and (37) articulate the voltage stress across C_2 and C_3, respectively. Similarly, Equations (38) and (39) elaborate on the voltage stress across C_4 and C_5. A noteworthy observation emerges from the calculations, indicating a significant reduction in voltage on the MOSFETs and diodes when the converter is tasked with supplying a load of 325 W. This reduction is particularly pronounced when L_3 and L_4 operate in DCM, while L_1 and L_2 function in CCM.

5. Features and Component Design of the Proposed Converter

In the development of the 325 W prototype for the converter, key components include capacitors, inductors, a gate drive circuit, power MOSFETs, and power diodes. The design of these components is crucial to validate the anticipated high voltage gain. Specifically, the proposed converter requires four small-value inductors and five small-value capacitors, with detailed parameter values available in Table 1. This table outlines essential prototype design parameters, forming a critical foundation for the successful implementation and verification of the converter's performance.

Table 1. Prototype component design for the proposed converter.

SiC MOSFETs	650 V 45 A Sw_1 1200 V, 35 A Sw_2
SiC Schottcky diodes	650 V 40 A
$L_1 = L_2$	150 uH, 3.3 mΩ
$L_3 = L_4$	100 uH, 2.9 mΩ

Table 1. *Cont.*

C_1	100 uF, 100 V
$C_2 = C_3$	100 uF, 330 V
$C_4 = C_5$	100 uF, 500 V
Cin	470 uF, 50 V
Vg	25–40 V
Vo	325–500 V
Power	325 W
D duty cycle	33% at 325 W, 500 V
Fs switching frequency	150 KHZ
Inductor size	(2.8 cm × 2.75 cm × 2.2 cm)
Ic drive circuit	1EDI60N12AF

The table above clearly indicates that the values of the inductors are exceptionally small, attributed to the utilization of a high switching frequency. Additionally, the internal resistance of the inductors is remarkably low, signifying a reduction in power losses for the proposed converter. To design the inductors for the proposed converter, Equation (40) guides the determination of the values for L_1 and L_2, while Equation (41) allows the calculation of the critical values for inductors L_3 and L_4. Equations (42) to (45) provide the values for C_1, C_2, C_3, C_4, and C_5, respectively. Examining the inductor specifications from Table 1, it is evident that the internal resistance of all inductors is minimal, attributed to the use of flat wire inductors with a ferrite core sized at (2.8 cm × 2.75 cm × 2.2 cm).

$$L_1 = \frac{VgDTs}{\Delta iL_1} = L_2 \tag{40}$$

$$L_{3Crit} = \frac{2VgDTs(1-D)}{Vo(1+D)} = L_{4Crit} \tag{41}$$

$$C_1 = \frac{4V_o(D+1)}{\Delta vc_1 R_L fs(1-D)} \tag{42}$$

$$C_2 = \frac{2Vo(D+1)}{\Delta vc_2 fsR_L(1-D)} = C_3 \tag{43}$$

$$C_4 = \frac{2V_oD(D+1)}{\Delta Vc_4.FsR_L(1-D)} \tag{44}$$

$$C_5 = \frac{V_oD}{\Delta V_oFsR_L} \tag{45}$$

6. Performance Comparison: Proposed Converter vs. Previous High-Boost Converters

A comparative analysis was undertaken between the proposed converter and prior DC-DC converters. The previous DC-DC converters were simulated in MATLAB Simulink under their specific conditions.

In Figure 5a, it can be observed that the MOSFET device in the proposed converter undergoes lower voltage stress at ultra-high voltage gain in contrast to the power MOSFET in previously studied converters. Additionally, Figure 5b illustrates that the voltage on the diode in the proposed converter is notably lower in comparison to the diodes in the converters from previous work. These findings underscore the enhanced performance and stress reduction achieved by the proposed converter in comparison to its counterparts at ultra-high voltage gain applications.

As illustrated in Figure 5c, it is evident that the proposed converter boasts a higher Mdc compared to previous boosting converters. Additionally, the proposed converter demonstrates superior Mdc even at very low duty cycles, specifically when D = 0.25. This implies that the proposed converter incurs lower switching and conduction losses, resulting in higher efficiency. Figure 5d shows that the voltage gain over the number of diodes in the proposed converter is higher compared with previous DC–DC converters.

In Figure 6a, it can be observed that the (Mdc/NL) voltage gain over the number of inductors in the proposed converter exhibits higher gain compared to previous converters. In Figure 6b, it is evident that the voltage gain over the number of switches (Mdc/Nsw) in the proposed converter shows higher gain compared to previous converters. In Figure 6c, it can be seen that the proposed converter has higher efficiency than previous works when the system operates in DCM at 500 V with a 250 W load at 96%. In Figure 6d, it can be observed that the proposed converter operates at a lower duty cycle than previous works. The proposed converter is capable of supplying 500 V at 325 W with a duty cycle of around 33%.

Table 2 presents a comprehensive comparison between the newly introduced converter and its predecessors. The analysis encompasses various critical factors, including the count of inductors, capacitors, diodes, switching frequency, input current, duty cycle percentage, and MOSFETs employed in both the innovative and traditional boosting converters. Notably, the proposed converter operates at a higher switching frequency, necessitating smaller inductors and capacitors while mitigating parasitic resistance. This design choice contributes to a more compact, lightweight, and cost-effective system. In contrast to its precursors, the proposed converter exhibits superior performance across efficiency, size, and cost-effectiveness metrics. While previous converters achieved the boost from low to high voltage ratios, they did so at the expense of a significantly high duty ratio. In contrast, the new converter adeptly elevates low voltage sources to variable output voltage levels spanning 325 V–500 V, requiring lower duty ratios than its predecessors. Additionally, the proposed converter incorporates fewer power diodes, thereby minimizing losses attributed to forward voltage and internal resistance in comparison to earlier models.

Furthermore, the innovative converter boasts a higher voltage gain relative to prior boosting converters, rendering it well suited for applications in renewable energy sources that demand variable and fixed high output voltage with a broader range in duty ratios. Impressively, it achieves an efficiency rating of 96%, underscoring its efficacy in energy conversion.

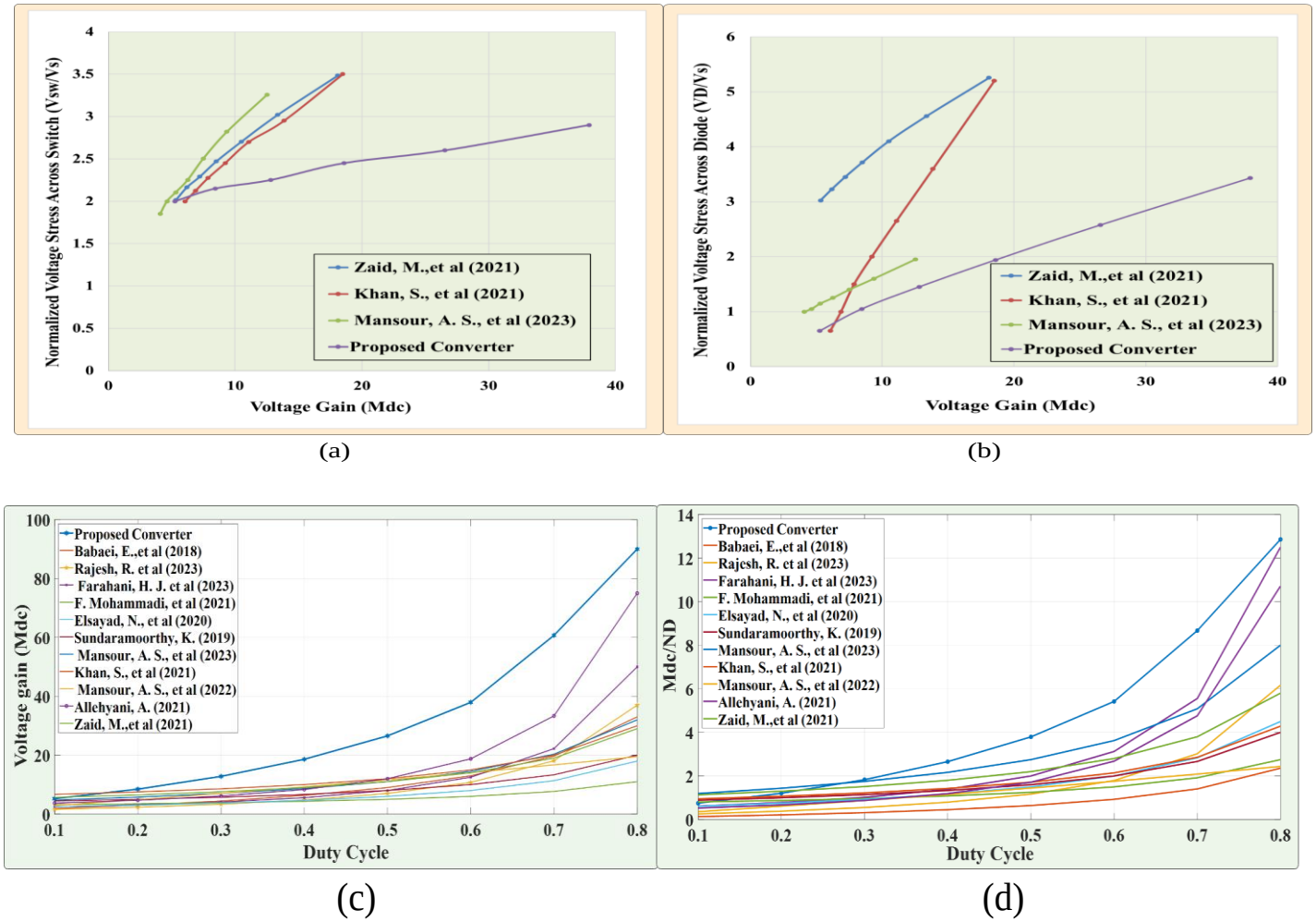


Figure 5. (**a**) Voltage stress across MOSFETs, Vsw/Vg vs. Mdc. (**b**) Voltage stress across diodes, VD/Vg vs. Mdc. (**c**) Comparisons of voltage gain, Mdc vs. D duty cycle. (**d**) Voltage gain Mdc/number of diodes (ND) vs. D.

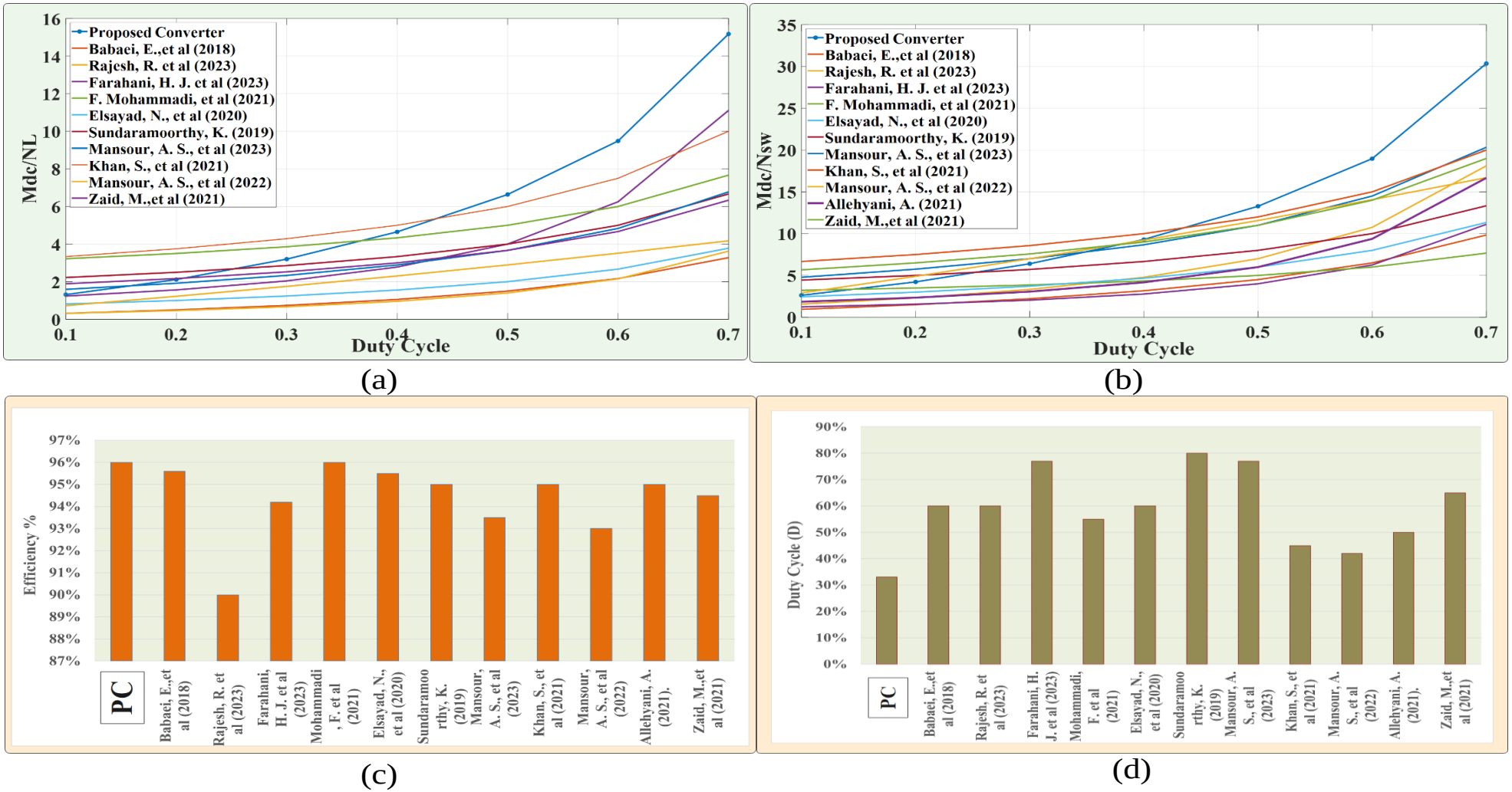


Figure 6. (**a**) Voltage gain Mdc/number of inductors (NL) vs. duty cycle. (**b**) Voltage gain Mdc/number of switches (NSW) vs. duty cycle. (**c**) Efficiency comparison of the proposed converter vs. previous work. (**d**) Duty cycle comparison of the proposed converter vs. previous work, where (PC) is the proposed converter.

Table 2. A comparison of the proposed converter with previous high-boosting converters.

Items	The Proposed Converter	Ref [3]	Ref [4]	Ref [8]	Ref [11]	Ref [13]	Ref [16]	Ref [19]	Ref [23]	Ref [26]	Ref [28]	Ref [31]
F_S (kHz)	150	20	50	100	50	100	20	5	50	1	31.3	100
Vg	25–40	20	20	15	10 v	300 v	24	24	16	24	20	30 v
Vo	325 v 500 v	160	200 v	384 v	50 v	800 v	350	107 v	150 v	221 v	200	200 v
L	4	6	5	2	1	3	2	3	2	4	2	3
C	5	1	8	4	4	7	4	4	5	2	5	4
Diode	7	14	6	4	4	4	5	4	7	8	7	5
Switches	2	2	1	2	1	1	1	1	1	2	1	2
Duty cycle	33%	60%	60%	77%	55%	60%	80%	77%	45%	42%	50%	65%
Power (w)	325	100	200	200	-	800	200	52	200	200	150	200
η%	96%	95.6%	90%	94.2%	96%	95.5%	95%	93.5%	95%	93%	95%	94.5%
$Mdc = \frac{Vout}{Vin}$	$\frac{(4+4D)}{(1-D)^2}$	$\frac{(1+7D)}{(1-D)}$	$\frac{1+3D-3D^2}{(1-D)^2}$	$\frac{2}{(1-D)^2}$	$\frac{(3-D)}{(1-D)}$	$\frac{(2+2D)}{(1-D)}$	$\frac{4}{(1-D)}$	$\frac{(4+3D)}{(1-D)}$	$\frac{6}{(1-D)}$	$\frac{(1+18.25D)}{(1-0.25D)}$	$\frac{(3-D)}{(1-D)^2}$	$\frac{(5+D)}{(1-D)}$
Mdc at D = 0.5	24	9	7	8	5	6	8	11	12	11.57	10	11

7. Control Strategy and State Space Equations

The controller for the proposed converter, as illustrated in Figure 7, employs a dual Proportional–Integral (PI) controller setup to enhance its operational efficiency. The first PI controller functions as an inner PI controller, ensuring the stability of the load current. Meanwhile, the second controller serves as an outer PI controller, responsible for maintaining the desired output voltage. The PI voltage controller operates by taking the difference between the target voltage and the actual output voltage as its input. Subsequently, it generates a reference current for the load based on this input. To prevent the converter from drawing excessive current, this reference current is deliberately limited. The disparity between the reference current and the actual current is then directed into the PI current controller, whose equation is denoted as (46). For optimal performance, it is essential to tune the Ki and Kp parameters of the controller. The output of the controller is input to the IC drive circuit used in the proposed converter (1EDI60N12AF). Each output of the IC drive provides pulses to the MOSFET. Additionally, both drives generate the same pulse for both the on and off states simultaneously. Notably, the parameters of the PI voltage controller should be set to be faster than those of the PI current controller. This ensures that the steady-state error is minimized and maintained at zero, contributing to the overall effectiveness of the control system.

$$U(t) = Kpe(t) + Ki\int e(t) \tag{46}$$

Upon implementing the recommended dual PI controller in the proposed converter to validate a consistent output voltage amidst varying input levels, Figure 7b unmistakably reveals that the converter maintains a steady 500 V output, even in the face of the input voltage reaching its lowest values. This implies that the proposed controller for the proposed converter is exceptionally reliable for applications requiring a consistently high output voltage. Moreover, it showcases the controller's adaptability across a broad range of duty ratios, contributing to higher power density in renewable energy applications.

Figure 7c provides a visual demonstration of the converter's capability to furnish a variable output voltage spanning from 300 V to 770 V while maintaining a fixed input voltage. Noteworthy is the converter's rapid response to changes, ensuring a swift and precise adjustment in the output voltage.

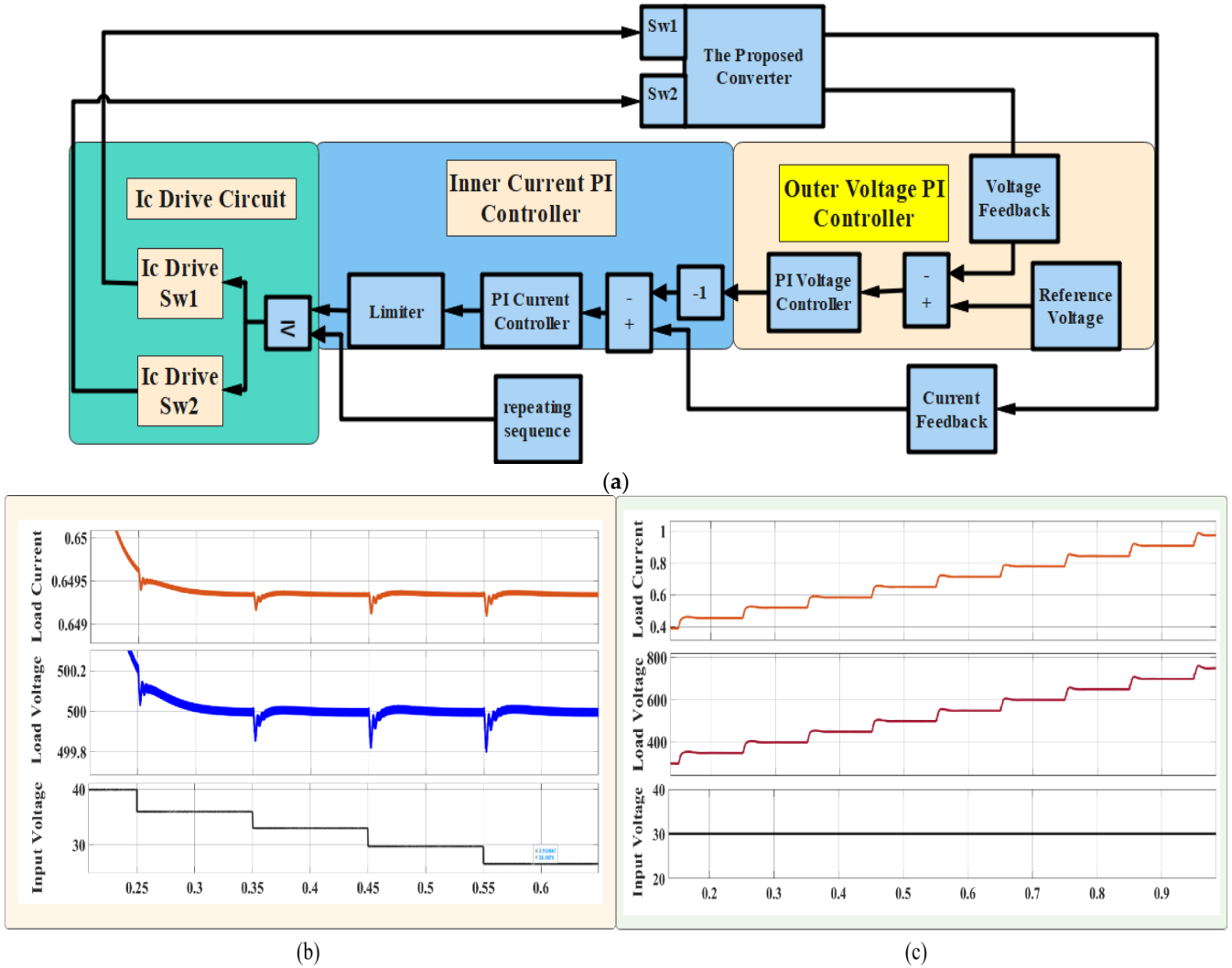


Figure 7. (**a**) Control strategy of the proposed converter; (**b**) output voltage of the proposed converter at variable input voltage; (**c**) variable output voltage at fixed input voltage.

This paper utilizes small signal modeling to assess the stability of the proposed open-loop converter. Two modes of operation are examined through the analysis of average state space modeling. The state space variables employed are the capacitor voltage and inductor current. The state space equations for the proposed converter under the CCM condition are derived as shown below, where X is the state variable, A is the state matrix, and B is the input matrix.

$$\left.\begin{array}{l} X = A1X + B1U/state \text{ variable during on state} \\ X = A2X + B2U/ \text{ state variable during off state} \\ X = (A1 + A2)X + (B1 + B2)U/state \text{ variable during on and off cycle} \end{array}\right\} \quad (47)$$

$$X = \begin{bmatrix} \frac{diL_A}{dt} \\ \frac{diL_B}{dt} \\ \frac{dVc_1}{dt} \\ \frac{dVc_2}{dt} \\ \frac{dVc_3}{dt} \\ \frac{dVc_4}{dt} \\ \frac{dVc_5}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_B} & \frac{1}{L_B} & 0 & 0 \\ \frac{4}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{2}{C_4} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_5RL} \end{bmatrix} \begin{bmatrix} iL_A \\ iL_B \\ Vc_1 \\ Vc_2 \\ Vc_3 \\ Vc_4 \\ Vc_5 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_A} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u \quad (48)$$

$$X = \begin{bmatrix} \frac{diL_A}{dt} \\ \frac{diL_B}{dt} \\ \frac{dVc_1}{dt} \\ \frac{dVc_2}{dt} \\ \frac{dVc_3}{dt} \\ \frac{dVc_4}{dt} \\ \frac{dVc_5}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{L_A} & \frac{-1}{L_A} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_B} & \frac{1}{L_B} & 0 & \frac{-1}{L_B} \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2C_2} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2C_3} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_4} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_5RL} \end{bmatrix} \begin{bmatrix} iL_A \\ iL_B \\ Vc_1 \\ Vc_2 \\ Vc_3 \\ Vc_4 \\ Vc_5 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_A} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u \quad (49)$$

$$X = \begin{bmatrix} \frac{diL_A}{dt} \\ \frac{diL_B}{dt} \\ \frac{dVc_1}{dt} \\ \frac{dVc_2}{dt} \\ \frac{dVc_3}{dt} \\ \frac{dVc_4}{dt} \\ \frac{dVc_5}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{(1-D)}{L_A} & \frac{-(1-D)}{L_A} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_B} & \frac{1}{L_B} & 0 & \frac{-(1-D)}{L_B} \\ \frac{(3D+1)}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{(1-D)}{2C_2} & \frac{D}{C_2} & 0 & 0 & 0 & 0 & 0 \\ \frac{(1-D)}{2C_3} & \frac{D}{C_3} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{(D+1)}{C_4} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_5RL} \end{bmatrix} \begin{bmatrix} iL_A \\ iL_B \\ Vc_1 \\ Vc_2 \\ Vc_3 \\ Vc_4 \\ Vc_5 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_A} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u \quad (50)$$

Equation (47) represents the state space equation during the on pulse cycle. Equation (48) represents the state space equation when the proposed converter is in the on state, while Equation (49) represents the state space equation in the off state. Equation (50) represents the state space equation of the proposed converter for one cycle. It can be seen that LA is considered to be the series connection of L_1 and L_2 in the on and off states, as both inductors have the same current. Additionally, LB is considered to be the series connection of L_3 and L_4 in the on and off states. This method simplifies the state space equation and facilitates the implementation of the control strategy; in short, the passive components are reduced when the state space equation is implemented.

8. Efficiency Calculation of the Proposed Converter

The proposed converter is comprised of two switches, seven diodes, five capacitors, and four inductors. It is crucial to note that these components deviate from ideal behavior. Specifically, each inductor possesses an internal resistance denoted as rl, while the capacitors exhibit equivalent series resistances represented by rc. The power diode introduces two types of power losses—firstly, from its internal resistance, and secondly, due to its forward voltage Vf. Additionally, power losses occur due to conduction and switching

losses associated with the power MOSFET devices. When evaluating the proposed converter, it is imperative to consider and account for all these losses. For a visual reference, Figure 8 illustrates both active and passive elements, including internal resistances. This provides a clear overview of the components and their associated resistances within the proposed converter.

$$Isw_{1rms} = \frac{4Io(1+D)\sqrt{D}}{(1-D)^2} \tag{51}$$

$$Isw_{2rms} = \frac{2I_o\sqrt{D}(1+D)}{(1-D)^2} \tag{52}$$

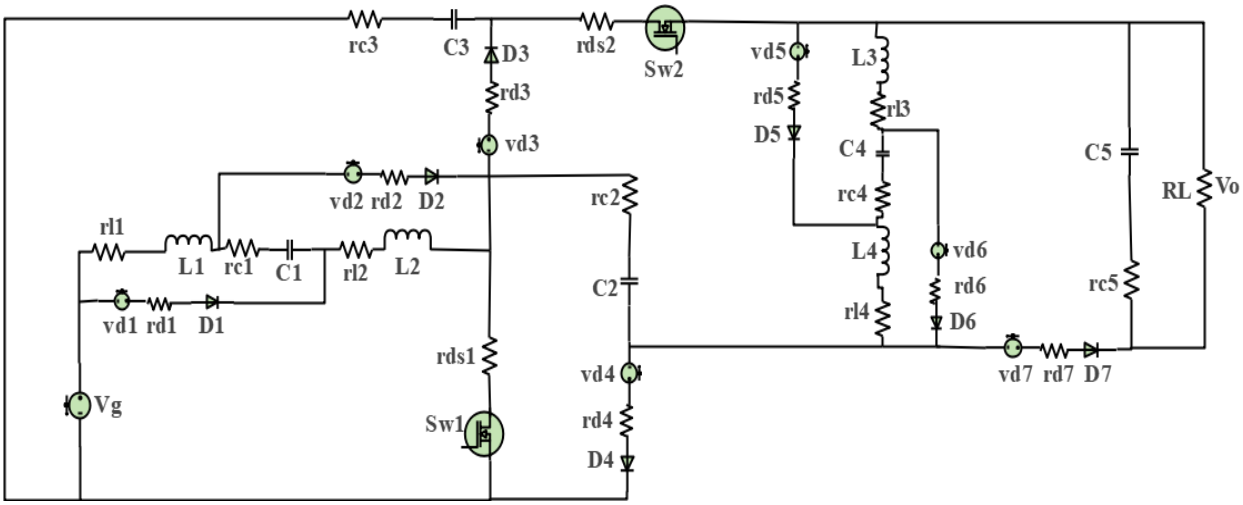


Figure 8. The Converter incorporated with all internal resistances of L, C, and power devices.

Equations (51) and (52) show the effective current that flows through Sw_1 and Sw_2, respectively.

$$I_{D_{1rms}} = \frac{2Io(1+D)\sqrt{D}}{(1-D)^2} \tag{53}$$

$$I_{D_{2rms}} = \frac{2Io(1+D)\sqrt{D}}{(1-D)^2} \tag{54}$$

$$I_{D_{3rms}} = \frac{Io(1+D)}{\sqrt{(1-D)^3}} = I_{D_{4rms}} \tag{55}$$

$$I_{D_{5rms}} = \frac{2I_o\sqrt{D}(1+D)}{(1-D)^2} = I_{D_{6rms}} \tag{56}$$

$$I_{D_{7rms}} = \frac{2I_o(1+D)}{\sqrt{(1-D)}} \tag{57}$$

Meanwhile, Equations (53) to (57) provide the effective currents passing through the power diodes.

$$iL_1rms = \frac{2I_o(D+1)}{(1-D)^2} = iL_2rms \tag{58}$$

$$iL_{3rms} = \frac{2Io(1+D)}{(1-D)} = iL_{4rms} \tag{59}$$

Additionally, Equations (58) and (59) describe the effective current flowing through inductors.

$$Ic_1rms = \frac{2I_o(D+1)}{(1-D)^2} \tag{60}$$

$$Ic_{2rms} = Ic_{3rms} = \frac{Io(1+D)\sqrt{3D+1}}{(1-D)^2} \tag{61}$$

$$Ic_{4rms} = \frac{2Io(1+D)}{(1-D)} \tag{62}$$

$$Ic_{5rms} = \frac{Io\sqrt{D-D^2+4(D+1)^2}}{\sqrt{(1-D)}} \tag{63}$$

Equations (60) to (63) present the effective current of capacitors C_1, C_2, C_3, C_4, and C_5, respectively.

8.1. Conduction and Switching Losses Calculation

$$P_{cd1} = \frac{16Po(1+D)^2D^2}{RL(1-D)^4}rds1 \tag{64}$$

$$P_{cd2} = \frac{4PoD^2(1+D)^2}{RL(1-D)^4}rds2 \tag{65}$$

$$P_{SW} = Vsw^2FsCo \tag{66}$$

$$P_{SWL1} = \frac{4Vg^2}{(1-D)^2}FsCo \tag{67}$$

$$P_{SWL2} = Vo^2 - \frac{16Vg^2}{(1-D)^2}FsCo \tag{68}$$

$$M_{TL} = \frac{16Po(1+D)^2D^2}{RL(1-D)^4}rds1 + \frac{4PoD^2(1+D)^2}{RL(1-D)^4}rds2 + \frac{2Vg^2FsCo}{(1-D)^2} + \frac{1}{2}(Vo^2 - \frac{16Vg^2FsCo}{(1-D)^2}) \tag{69}$$

Formulas (64) and (65) are utilized for computing power conduction losses in Sw_1 and Sw_2, identified as P_{cd1} and P_{cd2}, respectively. Equation (66) delves into the power switching losses of Sw_1 and Sw_2, denoted as $P_{SWL1,2,}$ with Co representing the output capacitor of the MOSFET and Fs representing the switching frequency. The cumulative power loss in the MOSFET devices, derived from Equation (69) as the summation of Formulas (64), (65), (67), and (68), is denoted as M_{TL}, encompassing the total power losses of the MOSFETs.

8.2. Losses in All Power Diodes

$$\left.\begin{array}{l} I_{D1ave} = \frac{2Po(D+1)D}{RL(1-D)^2} \\ I_{D2ave} = \frac{2Po(D+1)D}{RL(1-D)^2} \\ I_{D3ave} = I_{D4ave} = \frac{2Po(D+1)}{RL(1-D)} \\ I_{D5ave} = \frac{Po(1+D)D}{RL(1-D)} \\ I_{D6ave} = \frac{Po(1+D)D}{RL(1-D)} \\ I_{D7ave} = \frac{Po(1+D)}{RL(1-D)} \end{array}\right\} \tag{70}$$

$$\left.\begin{array}{l} P_{Dr} = IDrms^2 rd \\ P_{Dr1} = \frac{Po(1+D)^2 D}{RL(1-D)^4} rd1 \\ P_{Dr2} = \frac{Po(1+D)^2 D}{RL(1-D)^4} rd2 \\ P_{Dr3} = \frac{2Po(1+D)2}{RL(1-D)^3} rd3 \\ P_{Dr4} = \frac{2Po(1+D)2}{RL(1-D)^3} rd4 \\ P_{Dr5} = \frac{Po(1+D)^2 D}{RL(1-D)^4} rd5 \\ P_{Dr6} = \frac{Po(1+D)^2 D}{RL(1-D)^4} rd6 \\ P_{Dr7} = \frac{Po(1+D)^2}{RL(1-D)} rd7 \end{array}\right\} \quad (71)$$

$$\left.\begin{array}{l} P_{Vf} = I_{Dav} Vf \\ P_{Vf1} = Vf_1 \frac{2Po(D+1)D}{RL(1-D)^2} \\ P_{Vf2} = Vf_2 \frac{2Po(D+1)D}{RL(1-D)^2} \\ P_{Vf3} = Vf_3 \frac{2Po(D+1)}{RL(1-D)} \\ P_{Vf4} = Vf_4 \frac{2Po(D+1)}{RL(1-D)} \\ P_{Vf5} = Vf_5 \frac{Po(1+D)D}{RL(1-D)} \\ P_{Vf6} = Vf_6 \frac{Po(1+D)D}{RL(1-D)} \\ P_{Vf7} = Vf_7 \frac{Po(1+D)}{RL(1-D)} \end{array}\right\} \quad (72)$$

$$D_{TL} = P_{Dr1,2,3,4,5,6} + P_{Vf1,2,3,4,5,6} \quad (73)$$

Internal resistance losses (rd) and losses from the forward diode voltage (Vf) are considered the two main types of power loss in diodes. It is crucial to take into account all the power losses in the seven diodes of the proposed converter. To find the average current flowing through the diodes, Equation (70) is used. Using Equation (72) helps to identify losses from Vf, resulting in the power losses from the forward voltage (Pvf). On the other hand, Equation (71) sheds light on the diode power losses due to rd. Now, by adding up all these losses, we arrive at the total power losses (DTL) across the seven diodes. Equation (73) lays it all out, giving us a comprehensive view of the power losses in the diodes of the proposed converter.

8.3. Inductor and Capacitor Loss Calculation

$$\left.\begin{array}{l} P_L = iLrms^2 rl \\ P_{L1} = \frac{4Po(D+1)^2}{RL(1-D)^4} rl1 \\ P_{L2} = \frac{4Po(D+1)^2}{RL(1-D)^4} rl2 \\ P_{L3} = \frac{4Po(1+D)^2}{RL(1-D)^2} rl3 \\ P_{L4} = \frac{4Po(1+D)^2}{RL(1-D)^2} rl4 \end{array}\right\} \quad (74)$$

$$\left.\begin{aligned} P_C &= Icrms^2 rc1 \\ P_{C1} &= \frac{4Po(D+1)^2}{RL(1-D)^4} rc1 \\ P_{C2} &= \frac{Po(1+D)^2(3D+1)}{RL(1-D)^4} rc2 \\ P_{C3} &= \frac{Po(1+D)^2(3D+1)}{RL(1-D)^4} rc3 \\ P_{C4} &= \frac{4Po(1+D)^2}{RL(1-D)^2} rc4 \\ P_{C5} &= \frac{Po(D-D^2+4(D+1)^2)}{RL(1-D)} rc5 \end{aligned}\right\} \quad (75)$$

Formulas (74) and (75) facilitate the computation of power losses in the inductors (PL) and capacitors in the proposed converter, respectively. The converter incurs losses across MOSFETs, diodes, inductors, and capacitors. The aggregate power loss (TPLPC) of the converter, as outlined in Equation (76), amalgamates power losses in power MOSFETs (MTL), total diode losses (DTL), and losses in all inductors (ITL) and capacitors (CTL). Efficiency, a pivotal gauge of a converter's effectiveness, is determined by Equation (77). It is worth noting that opting for SiC MOSFETs with minimal on-state resistance proves advantageous in curtailing conduction losses. Furthermore, employing low-value inductors with exceptionally low internal resistance contributes to augmenting the overall efficiency and performance of the proposed converter.

8.4. Total Power Losses in the Proposed Converter

$$T_{PLPC} = M_{TL} + \mathrm{D_{TL}} + \mathrm{I_{TL}} + \mathrm{C_{TL}} \quad (76)$$

$$\eta = \frac{P_o}{P_o + T_{PLPC}} 100\% \quad (77)$$

9. Results and Discussions

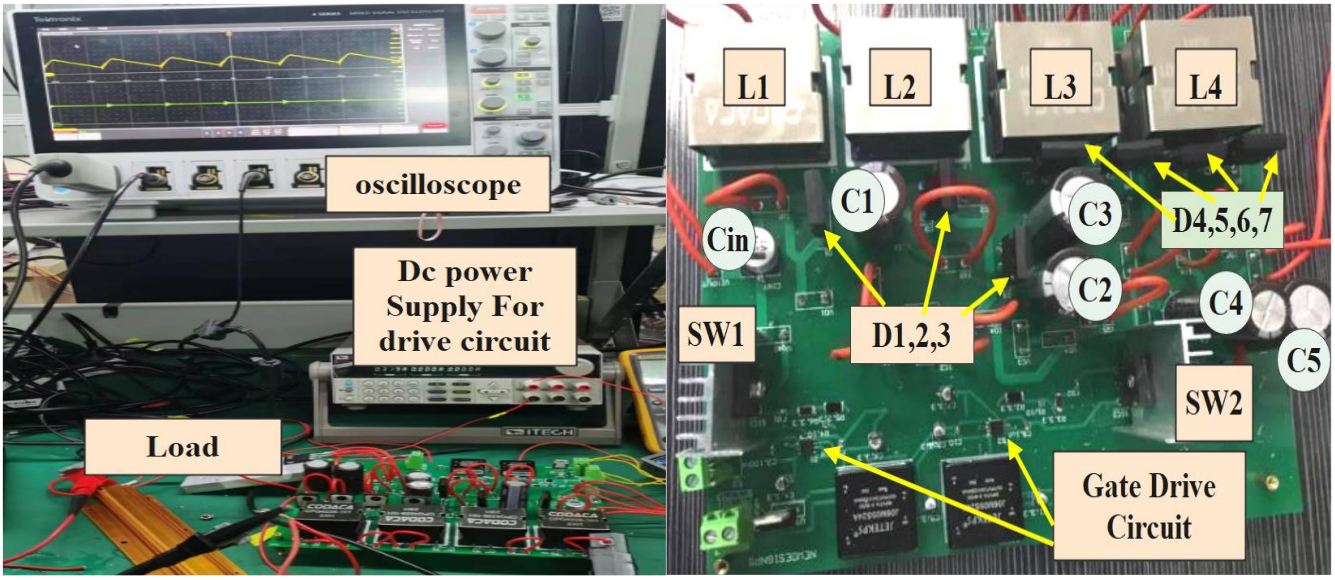
Our focus was on validating the experimental results presented in Figure 9b, and to accomplish this, we designed a 325 W PCB prototype. We conducted rigorous experimental tests on the proposed converter in a laboratory setting, as illustrated in Figure 9a. This real-world testing allowed us to gather practical data and evaluate the converter's performance. To further validate our findings and ensure robustness, we utilized simulation tools such as MATLAB Simulink and PLECS software. These software platforms enabled us to simulate and verify the experimental results in various scenarios, providing additional evidence of the converter's effectiveness. In our design and analysis process, we also accounted for the parasitic resistance associated with the inductors and capacitors in the converter. Recognizing the impact of these parasitic elements on the overall system performance, we incorporated their effects into our evaluations and made necessary adjustments to enhance the accuracy of our results. By combining practical experimentation, simulation tools, and careful consideration of parasitic elements, we aimed to establish the reliability and validity of the proposed converter design. These comprehensive validation efforts reinforce the credibility of our experimental results and contribute to the overall confidence in the performance of the converter.

In Figure 10a, it can be seen that the output voltage is 500 V at Vg = 25 V and a load current of 0.65 A with a gain Mdc = 20. In Figure 10b, V_{C1} is equal to 29 V, which matches Vg. V_{C2} and V_{C3} are both 84.7 V, calculated using Equation (36). Additionally, V_{C4} can be observed to be equal to 169.18 V when the converter supplies a 500 V output voltage at 325 W. V_{C5}, equal to the output voltage, is also shown. In Figure 10c, the voltage across the diodes is substantially reduced, resulting in a reduction in total power loss in the proposed converter (T_{PLPC}). Moreover, voltage across diodes VD_5, VD_6, and VD_7 is significantly reduced when the converter supplies 325 W at Vo = 500 V, where the MHSLCP inductors L_3 and L_4 operate in DCM. Figure 10d represents the current through the capacitors, while

Figure 10e displays the current through the diodes. D_7 operates at zero current when the MHSLCP inductors operate in DCM and the converter supplies 325 W at 500 V. Figure 10f shows the current through the inductors, where the MHSLCP inductors operate in DCM and the converter supplies 325 W at 500 V.

In Figure 11a, the VL is visible, where the voltage across L_1 and L_2 is equal to Vg, and the VL_3 and VL_4 are almost equal to MSC voltage. VL_3 and VL_4 are significantly reduced at Vo = 500 V at 325 W. Figure 11b shows the current through inductors when the proposed converter operates in CCM. Figure 11c displays Vo = 334 V and Io = 1 A at Vg = 30 V with D = 28%. Figure 11d shows Vo = 500 V and Io = 0.65 A at Vg = 30 V with D = 31%. Figure 12e reveals the Isw1 and Isw2, where the current through Sw2 is significantly lower, reducing the conduction loss of the power MOSFET. Furthermore, the Vsw_2 is significantly reduced when the converter supplies a 500 V output at 325 W. Moreover, the voltage across Sw_1 is also low at Vo = 500 V. Figure 11f shows Vo = 500 V and Io = 0.66 A at Vg = 40 V with D = 26%.

Regarding the experimental results, Figure 12a displays the current through inductors L_1 and L_2, along with V_{C3}. In Figure 12b, the current through inductors L_3 and L_4 during operation in DCM is visible. Figure 12c illustrates the current through Sw_1 and Sw_2. In Figure 12d, V_{C4} is 87 V. Figure 12e presents VD_1 and VD_2, while Figure 12f demonstrates VD_3 and VD_4 at Vs = 30 V and ID_3 and ID_4. Figure 13a exhibits VD_7, and Figure 13b shows Vsw_1, which was found to be a small value. In Figure 13c, Vsw2 is illustrated for the time interval (D < t < D1), which is a very short duration, and (D1 < t < Ts), where it equals Vc_3. In Figure 13d, VD_5 and VD_6 are reduced when the converter supplies Vo = 500 V at 325 W. Figure 13e shows the load current Io = 1 A at Vo = 325 V and 325 W. Furthermore, Figure 13f displays a load current of 0.65 A at Vo = 500 V and 325 W. Additionally, in Figure 13f, it can be observed that the input current (Iin) has no pulsation after adding a very small input capacitor (Cin). In Figure 13g, the current through D_1, D_2, D_3, and D_4 is depicted, while Figure 13h represents the current through the capacitors C_1 and C_4.



(a) (b)

Figure 9. (**a**) Experimental 325 W prototype of the proposed converter; (**b**) 325 W PCB prototype of the PC.

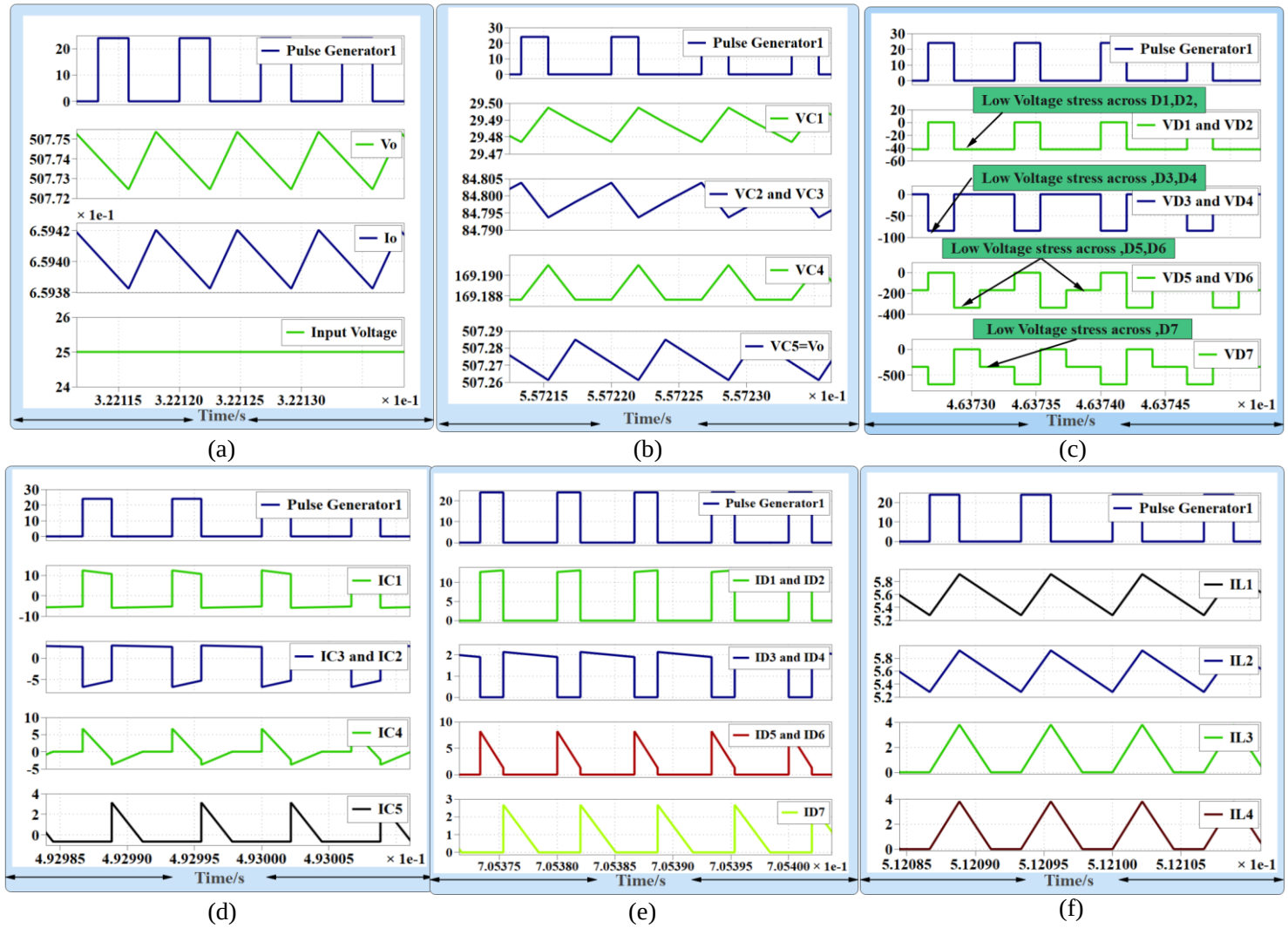


Figure 10. (**a**) Vo, Io, Vg; (**b**) V_{C1}, V_{C2}, V_{C3}, V_{C4}, Vc_5; (**c**) VD_1, VD_2, VD_3, VD_4, VD_5, VD_6, VD_7; (**d**), IC_1, IC_2, IC_3, IC_4, IC_5; (**e**) ID_1, ID_2, ID_3, ID_4, ID_5, ID_6, ID_7; (**f**) IL_1, IL_2, IL_3, IL_4.

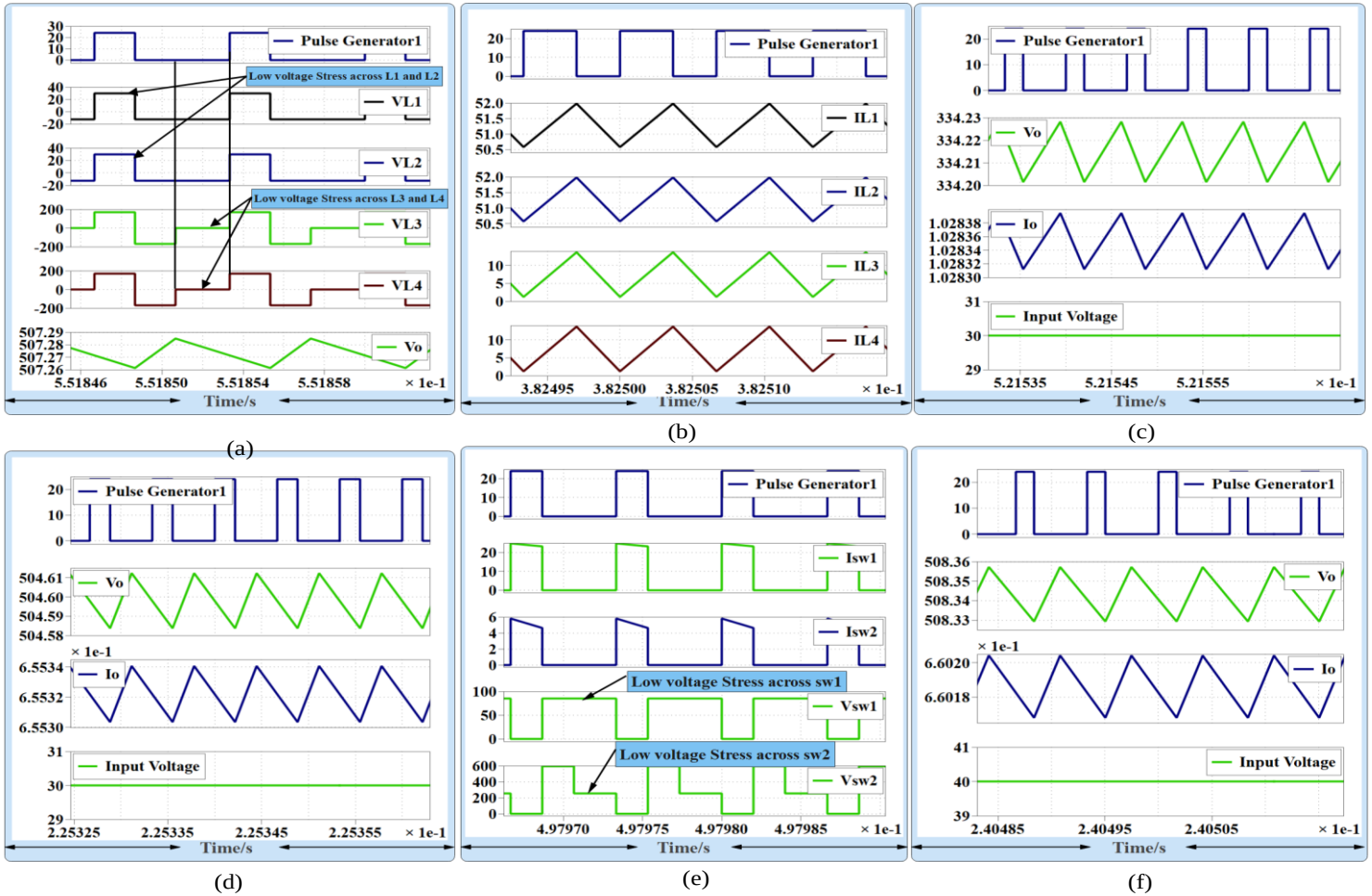


Figure 11. (**a**) VL_1, VL_2, VL_3, VL_4; (**b**) IL_1, IL_2, IL_3, and IL_4 in CCM; (**c**) Vo, Io, Vg; (**d**) Vo, Io, Vg; (**e**) Isw_1, Isw_2, Vsw_1, Vsw_2; (**f**) Vo, Io, Vg.

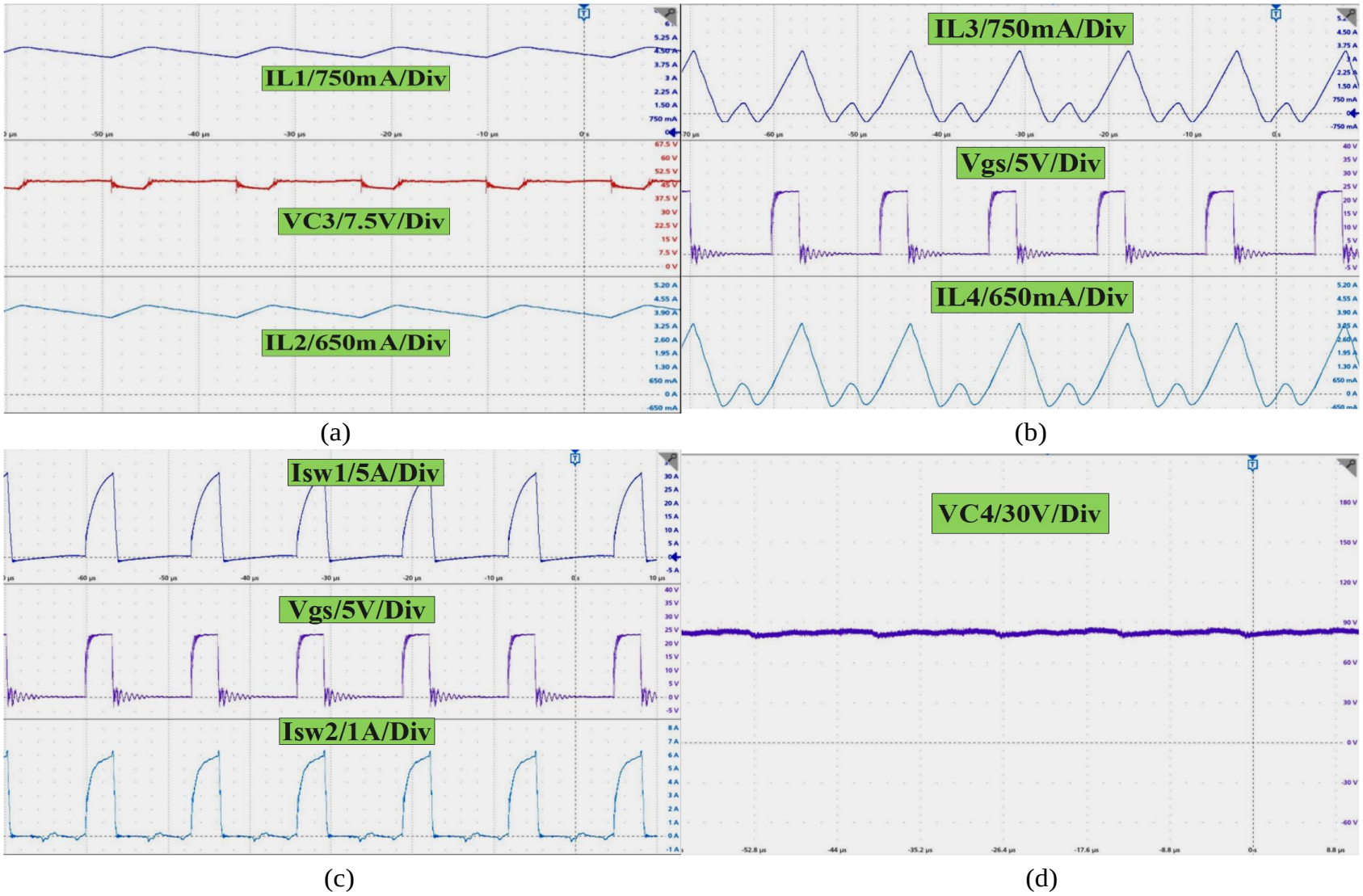
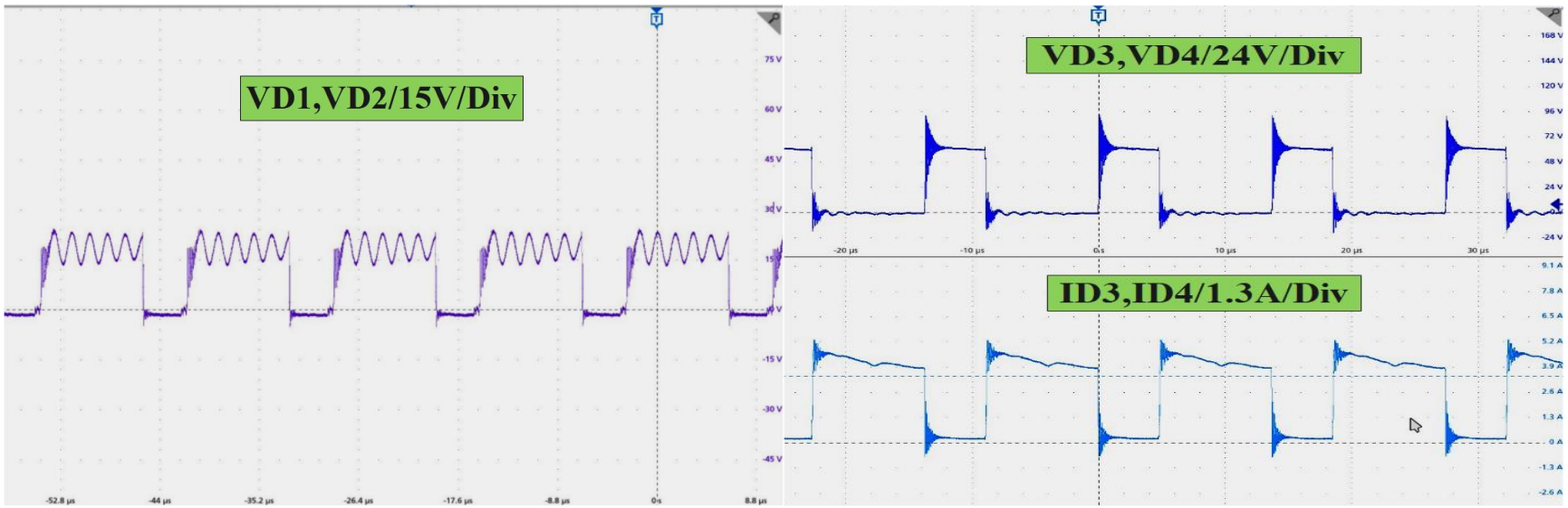


Figure 12. *Cont.*



(e) (f)

Figure 12. (**a**) IL_1, IL_2, VC_3; (**b**), IL_3, IL_4, Vgs; (**c**), Isw_1, Isw_2, Vgs; (**d**) VC_4; (**e**) VD_1, VD_2; (**f**) VD_3, VD_4, ID_3, ID_4.

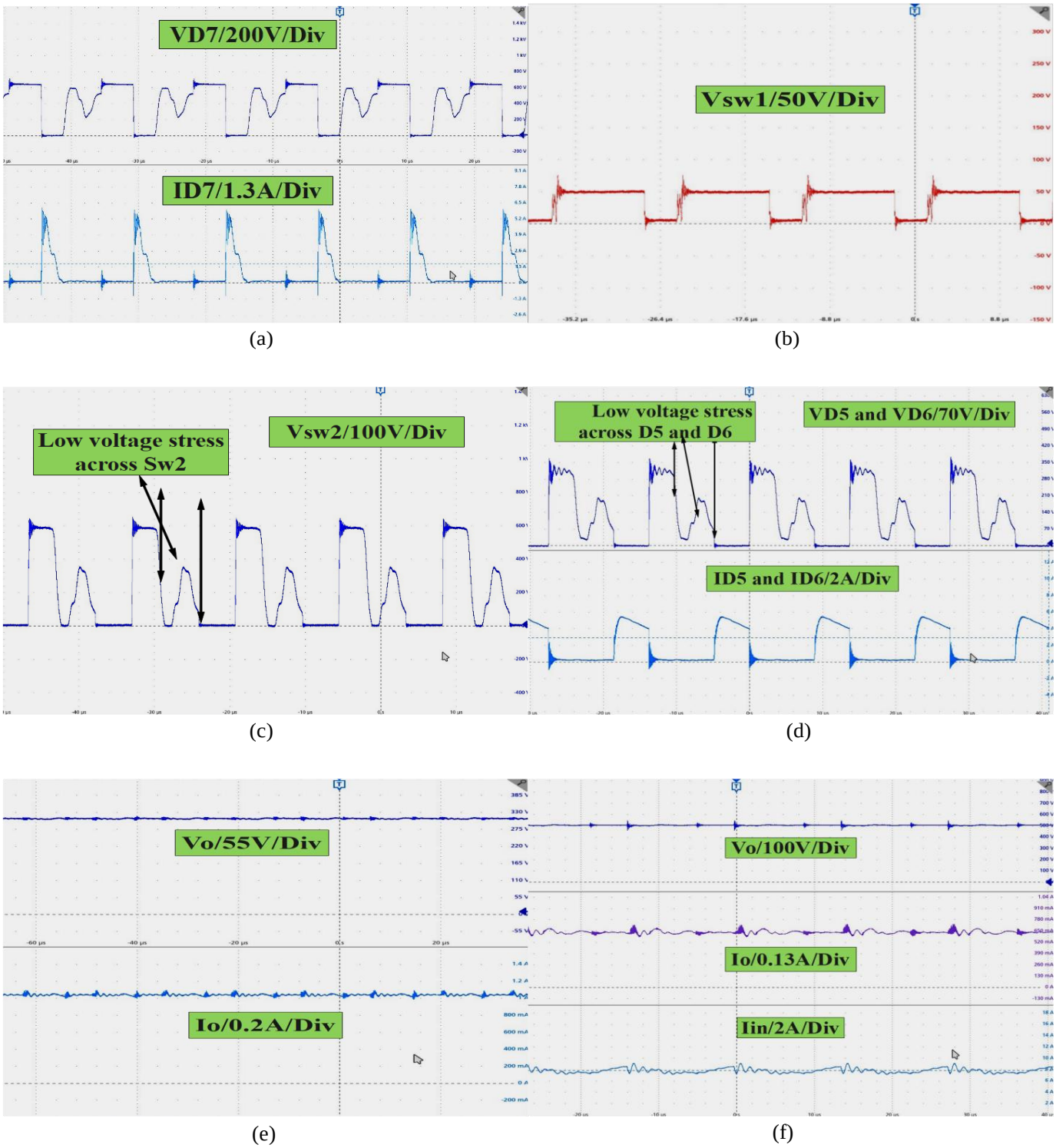
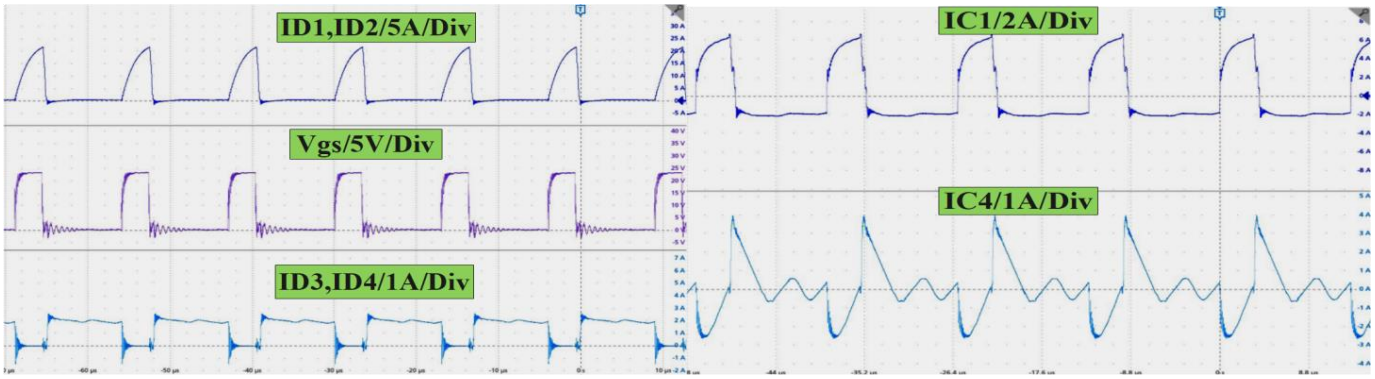


Figure 13. *Cont.*



(g) (h)

Figure 13. (**a**) VD_7, ID_7; (**b**), Vsw_1; (**c**) Vsw_2; (**d**) VD_5, VD_6.ID_5, ID_6; (**e**) Io = 1 A at Vo = 325 V; (**f**) Io = 0.65 A, Vo = 500 V, 325 W, Iin; (**g**), ID_1, D_2, D_3, D4; (**h**) IC_1, IC_4.

It is evident that the converter can step up a low input voltage to a high output voltage from (30 to 500 V) at a very low duty cycle. Moreover, a low duty cycle at high voltage gain (Mdc) significantly reduces the total power losses of the converter, enabling it to operate with high efficiency and performance. Additionally, the MHSLCP inductors operate in DCM when the converter supplies 500 V. Furthermore, the voltage on diodes, inductors, and MOSFETs is greatly reduced at high voltage gain when the MHSLCP inductors operate in DCM. In addition, the proposed converter operates in DCM at high voltage gain under high load power to increase efficiency and performance, following voltage stress reduction on power devices.

In Figure 14a, it is evident that the proposed converter achieves high efficiency, reaching 96.2% at a very low duty cycle at Vo = 500 V. Figure 14b shows that the converter at a very low duty cycle can supply a high load current at the high efficiency of 96%. In Figure 14c, the total power losses of the proposed converter at Vo = 500 V and 325 W load are depicted. Notably, high losses are attributed to diodes, which are significantly reduced after implementing SiC diodes with very low forward voltage and low internal resistance. Additionally, lower losses were observed in inductors after using flat wire inductors with very low internal resistance at a very high switching frequency. Figure 14d illustrates the percentage of losses of elements of the converter at 325 W and Vo = 500 V. Diodes contributed the highest losses, accounting for almost 43% of all losses.

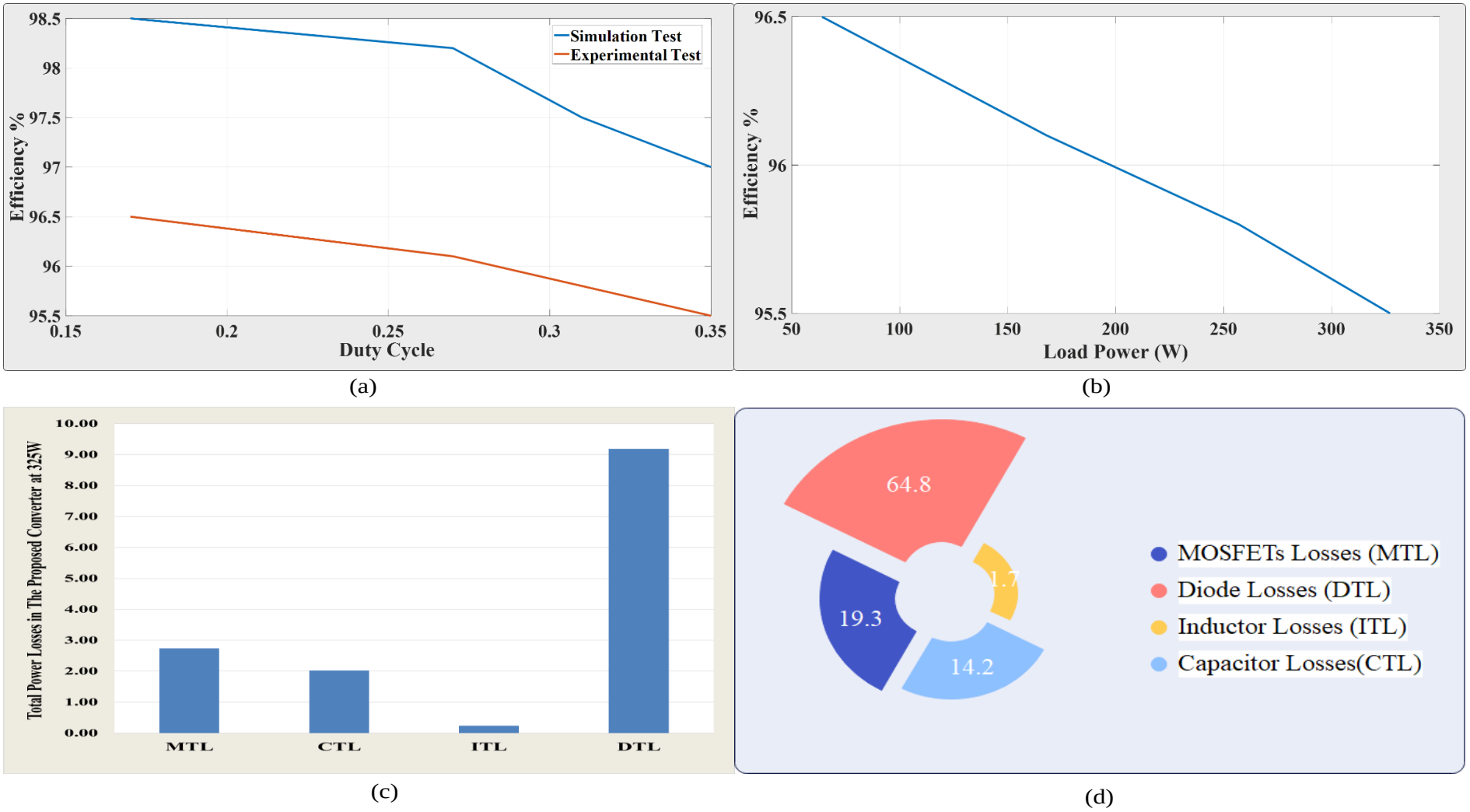


Figure 14. Efficiency of the proposed converter (**a**) vs. duty cycle and (**b**) vs. load power watts; (**c**) (T_{PLPC}) at 325 W and 500 V output voltage; (**d**) percentage losses of the elements in the converter at 325 W.

10. Conclusions

In conclusion, this paper has presented a high-efficiency DC-DC converter utilizing the interleaved configuration of the MHSLCS with an MSC and MHSLCP. The primary objective of achieving exceptionally high voltage gain in photovoltaic applications has been successfully validated through the incorporation of the MHSLCS with an MSC interleaved with the main switch, effectively doubling the voltage transfer gain. The inclusion of the MHSLCP as interleaved components, integrated in parallel with an auxiliary switch, not only optimizes voltage transfer gain but also ensures low voltage stress across the auxiliary switch, achieved by combining the main and auxiliary switches with the MSC. Furthermore, the series connection of each pair of inductors, with matching voltage and current, serves to reduce the number of passive elements and enhance the overall performance of the proposed converter. The inductors of the MHSLCP operating in DCM (discontinuous conduction mode) contribute to significant stress reduction in power diodes and switches at high output voltage, thereby improving overall efficiency. The converter's operation at high efficiency is particularly pronounced when the inductors of the MHSLCP operate in DCM, leading to a substantial reduction in voltage stress across power switches and diodes during high-power applications. Moreover, the use of only one input capacitor eliminates pulsations in input current at both low and high duty ratios. The implementation of a dual PI controller as the control strategy has proven effective, demonstrated by the converter achieving a high efficiency of 96.2% at a low duty cycle and a 500V output voltage. The comprehensive analysis of power losses underscores the significance of employing SiC diodes and flat wire inductors, contributing to an overall efficiency improvement. The converter's ability to operate at a low duty cycle and step up low input voltage to high output voltage highlights its efficiency, emphasizing the crucial role of key components in reducing power losses and enhancing overall performance.

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