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# Active Clamp Boost Converter with Blanking Time Tuning Considered

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**Abstract:** An active clamp boost converter with blanking time auto-tuned is presented herein, and this is implemented by an additional auxiliary switch, an additional resonant inductor, and an additional active clamp capacitor as compared with the conventional boost converter. In this structure, both the main and auxiliary switches have zero voltage switching (ZVS) turn-on as well as the output diode has zero current switching (ZCS) turn-off, causing the overall efficiency of the converter to be upgraded. Moreover, as the active clamp circuit is adopted, the voltage spike on the main switch can be suppressed to some extent whereas, because of this structure, although the input inductor is designed in the continuous conduction mode (CCM), the output diode can operate with ZCS turn-off, leading to the resonant inductor operating in the discontinuous conduction mode (DCM), hence there is no reverse recovery current during the turn-off period of the output diode. Furthermore, unlike the existing soft switching circuits, the auto-tuning technique based on a given look-up table is added to adjust the cut-off time point of the auxiliary switch to reduce the current flowing through the output diode, so that the overall efficiency is upgraded further. In this paper, basic operating principles, mathematic deductions, potential designs, and some experimental results are given. To sum up, the novelty of this paper is ZCS turn-off of the output diode, DCM operation of the resonant inductor, and auto-tuning of cut-off time point of the auxiliary switch. In addition, the efficiency of the proposed converter can be up to 96.9%.

**Keywords:** active clamp; auto-tuning; boost converter; ZCS; ZVS; FPGA; PWM



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## 1. Introduction

How to obtain a high-power density power supply is becoming more and more attractive in the world. By increasing the switching frequency, the size of magnetic devices and capacitors can be reduced so that high-power density requirements can be achieved. However, for the hard switching to be considered, the higher the switching frequency, the greater the switching loss and the more difficult the heat process. In addition, the switching loss under hard switching is proportional to the switching frequency. Consequently, the problem in high switching frequency is becoming more and more serious, thereby causing resonant and soft-switching converters to develop to reduce the switching loss.

The conventional resonant converter is based on the inductor connected in series with the main switch or the capacitor connected in parallel with the main switch so as to form a resonant loop. As the voltage on or current in the switch is dropped to zero, the switch is switched to achieve zero voltage switching (ZVS) turn-on of the switch or zero current switching (ZCS) turn-off of the switch. Basically, this method can reduce the crossover area of voltage and current of the switch, thereby decreasing the switching loss. However, large voltage and current spikes increase the voltage and current stresses of switches as well as increase the conduction losses. Furthermore, in order to render the output voltage

controlled at a desired value, the switching frequency is varied because the resonant time is fixed, causing the design of the filter to be difficult.

As the conventional resonant converter has the demerits mentioned above, the soft-switching converter is presented. The ZVS/ZCS pulse-width-modulation (PWM) converter [1–3] has put an auxiliary switch to the resonant loop of the resonant converter to make the resonant time point adjustable, thereby leading to fixed frequency control and making the design of the filter easy. However, the conduction loss is large because the resonant voltage on and current in the circuit elements are large. The operating principle of the ZVT/ZCT converter is that prior to turn-on of the main switch, the auxiliary switch is conducted, and hence the transient resonance occurs. As the voltage on or current in the main switch resonates to zero, the main switch is turned on to achieve ZVT turn-on or ZCT turn-off. As the auxiliary switch in the off-state, no resonance happens, leading to effectively reducing the voltage or current stress as well as conduction loss. In the literature [4,5], although the main switches have ZVS turn-on, the auxiliary switches still operate under hard switching. In the literature [6–8], although the main and auxiliary switches have ZVS turn-on, many components lead to an increase in cost. The operating behavior of the ZVZCT converter [9–11] is that the auxiliary switch has two transient resonances over one cycle so that the main switch has ZVT turn-on and ZCT turn-off. Indeed, this converter can reduce switching and conduction losses, and no additional voltage and current stresses on components. However, such a converter has complexity in control and a relatively large part count, leading to an increase in cost. Furthermore, as the ZVS or ZVT turn-on is relatively suitable for the metal-oxide-semiconductor field-effect transistor (MOSFET) switch [10], there are many studies on the MOSFET switch with ZVS or ZVT turn-on.

In addition, based on the above-mentioned, the ZVS pulse width modulation (PWM) converter, the ZVT converter, and the ZVZCT converter have individual disadvantages. Accordingly, the active clamp technique is developed, which is composed of an auxiliary switch in series with a capacitor. The work of [12] applies the synchronous rectifier to the ZVS active clamp forward converter to reduce the conduction loss. Another paper [13] applies the soft-switched synchronous rectifier to the ZVS active clamp forward converter to reduce the conduction loss as well as the switching loss. A further paper [14] applies the two-switch active clamp to a forward converter for high input voltage applications. The work of [15] applies the phase-shift control to the dual active clamp forward converter to reduce the conduction loss. The work of [16] utilizes the combination of active clamp and passive clamp to improve the light-load efficiency. A further paper [17] applies the secondary-side resonance scheme to the active clamp flyback converter to shape the primary-side current waveform, and hence to reduce the primary-side root-mean-square (RMS) value. Another paper [18] employs the primary-side digital control to regulate the active lamp flyback converter. The work of [19] applies the bidirectional concept to the ZVT active clamp boost converter. The work of [20] applies a coupled inductor to the ZVS active clamp boost converter. In the work of [21], the improved ZVS topology is applied to the active clamp buck converter. Although the converters shown in [19–21] have ZVS or ZVT turn-on of the main switches, the number of components used is large, leading to an increase in cost as well as difficulty in circuit analysis. In addition, in CCM, there is no ZCS turn-off of the output diode, leading to a problem in reverse recovery current created from the output diode, which operates during the turn-off period.

Based on the aforementioned, in this paper, one traditional boost converter along with one auxiliary circuit is presented. This auxiliary circuit is composed of one auxiliary switch, one resonant inductor, and one active clamp capacitor, so that the main switch and the auxiliary switch are turned on with ZVS and the output diode is turned off with ZCS, thereby resulting in upgrading the overall efficiency. Furthermore, the proposed active clamp has a function of voltage clamp, thereby leading to reducing the voltage spike on the main switch to some extent, whereas this structure can also cause the output diode to have ZCS turn-off, thereby removing the reverse recovery current. Above all, the proposed auto-tuning technique of the second blanking time is applied to the proposed circuit to

upgrade the overall efficiency further. By the way, the potential application of the proposed soft switching converter is for high-power light-emitting diode (LED) lighting fed by the direct current (DC) voltage to improve the overall efficiency [22].

## 2. Methodology

### *2.1. Proposed Converter*

Figure 1 displays the proposed active clamp boost converter, which is constructed by one conventional boost converter combined with one auxiliary circuit. The former is built up by one input inductor $L_{in}$ and one main switch $S_1$, along with one body diode $D_{s1}$, one parasitic capacitor $C_{s1}$, one output diode $D_o$, and one output capacitor $C_o$. The latter is constructed by one auxiliary switch $S_2$ along with one body diode $D_{s2}$, one parasitic capacitor $C_{s2}$, one resonant inductor $L_r$, and one active clamp capacitor $C_c$. The load is represented by one output resistor $R$. In addition, Figure 2 displays the equivalent circuit of the circuit shown in Figure 1, based on the assumption that the values of $C_o$ and $C_c$ are large enough to be regarded as ideal voltage sources, whereas the value of $L_{in}$ is large enough to be viewed as an ideal current source.

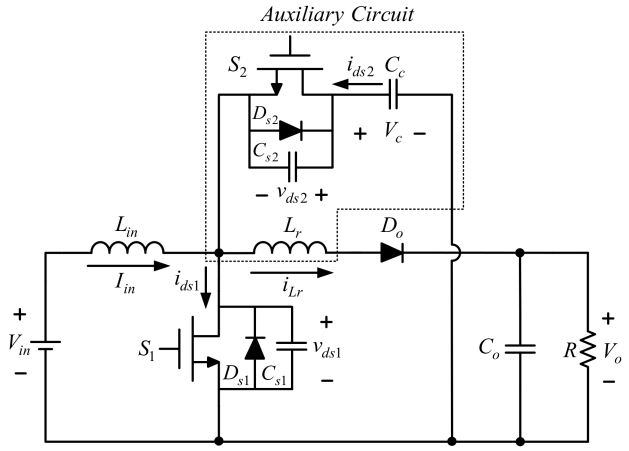


**Figure 1.** Proposed active clamp boost converter.

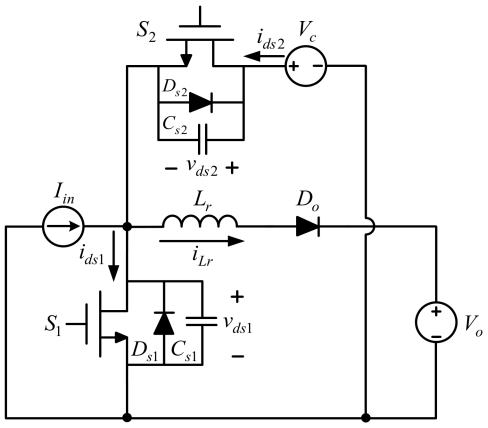


**Figure 2.** Equivalent circuit of the circuit shown in Figure 1.

### *2.2. Operation Principles*

#### 2.2.1. Circuit Behavior

Prior to this section, the symbols and assumptions associated with the circuit displayed in Figures 1 and 2 are given as follows: (i) $V_{in}$, $V_o$, and $V_c$ are the dc input voltage, dc output voltage, and the dc voltage clamp voltage, respectively; (ii) $I_{in}$ is the dc input current; (iii) $i_{Lr}$ is the current in $L_r$ and $D_o$; (iv) $v_{ds1}$ and $i_{ds1}$ are the voltage on and current in $S_1$,

respectively; (v) $v_{ds1}$ and $i_{ds2}$ are the voltage on and current in $S_2$, respectively; and (vi) all the elements are ideal except that switches have individual body diodes and parasitic capacitors. There are nine stages in the converter operating shown in Figure 3, where $t_{on}$ is the turn-on time of $v_{gs1}$, which is equal to $DT_s$ with a switching period of $T_s$ and a duty cycle of $D$, whereas $t_{off}$ is the turn-off time of $v_{gs1}$, which is equal to $(1-D)T_s$.

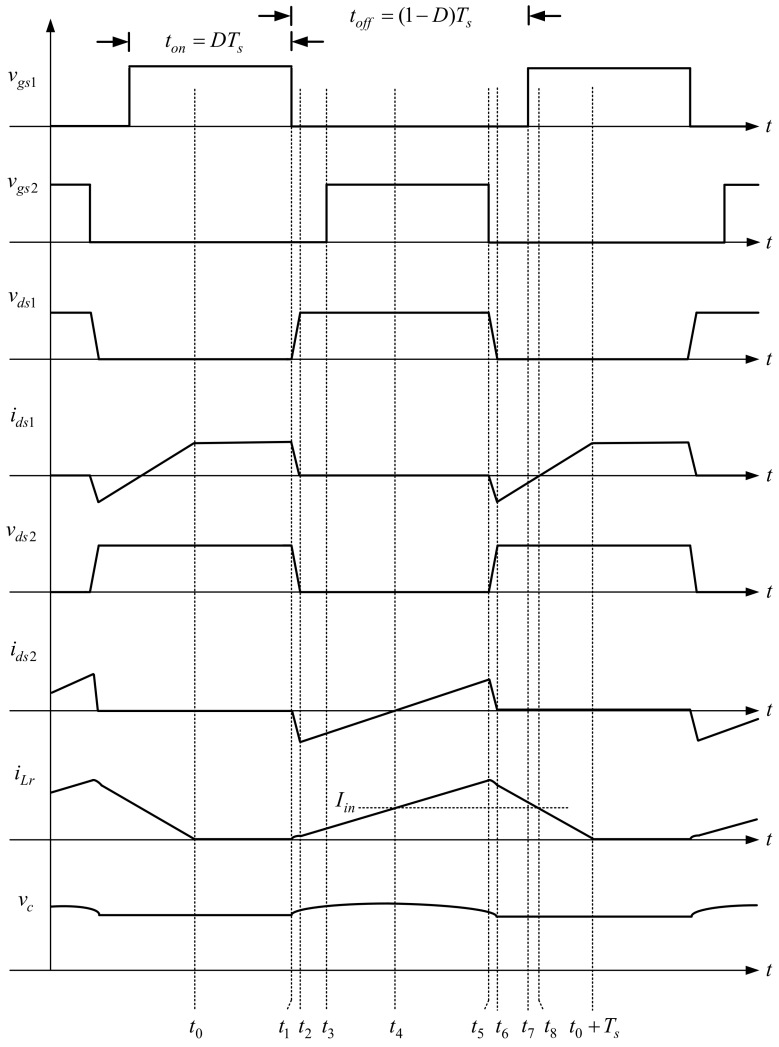


**Figure 3.** Key waveforms pertaining to the working converter.

Stage 1: $(t_0 \leq t \leq t_1)$

As illustrated in Figures 3 and 4, $S_1$ is ON but $S_2$ is OFF. During this stage, $L_{in}$ is magnetized by $V_{in}$. At the same time, $v_{ds2}$ is clamped at $V_c$. Once $S_1$ is cut off, the operation moves to stage 2.

Stage 2: $(t_1 \leq t \leq t_2)$

As illustrated in Figures 3 and 5, $S_1$ is cut off and $S_2$ is still OFF. During this state, $C_{s1}$ is abruptly charged to $V_c$. As $V_c = v_{ds1} + v_{ds2}$, $C_{s2}$ is abruptly discharged to zero. At the same time, $L_r$ is magnetized and the energy at input terminal is transferred to the output terminal via $D_o$. Once the energy stored in $C_{s2}$ is entirely exhausted, the operation proceeds to stage 3.

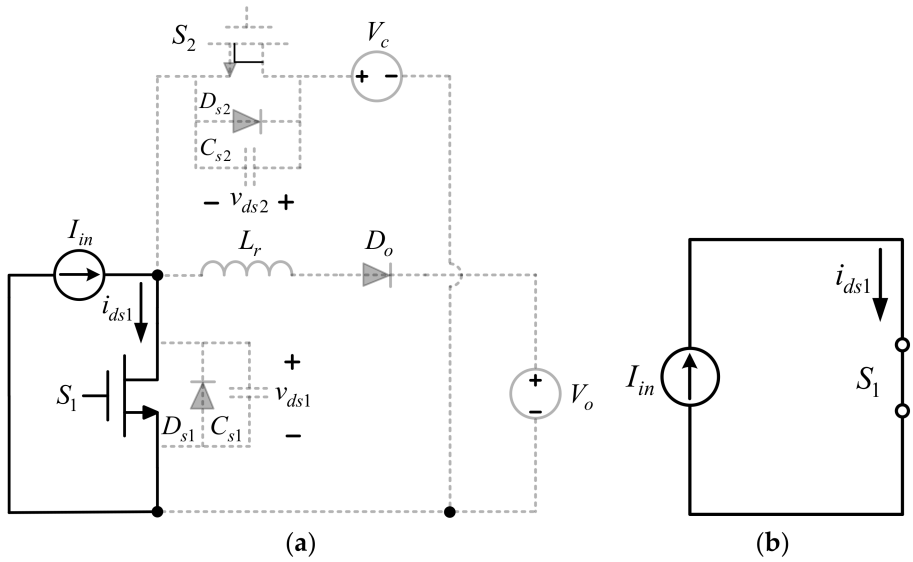


**Figure 4.** (**a**) Current path for stage 1; (**b**) equivalent of (**a**).

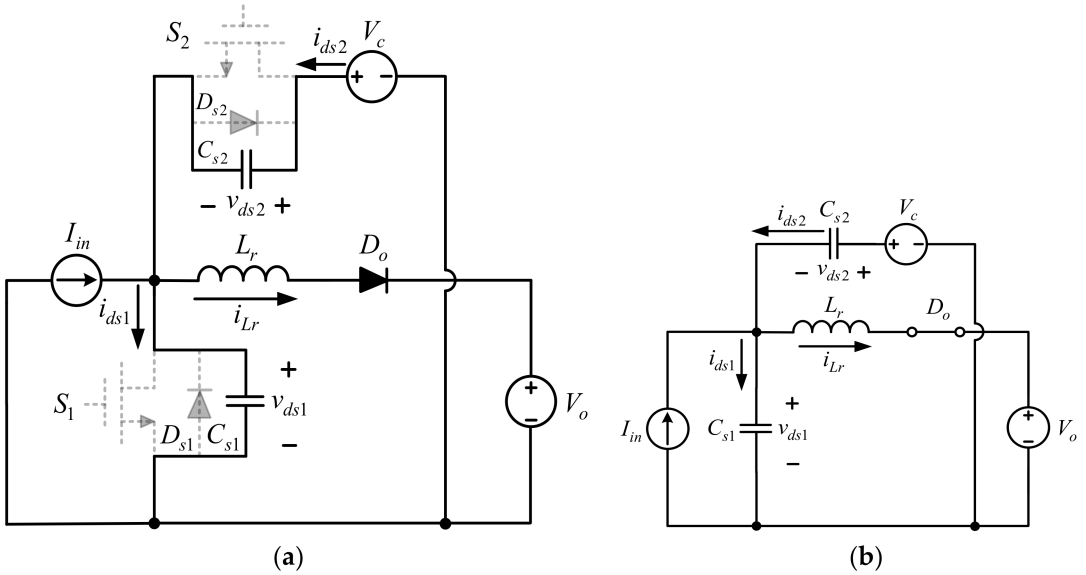


**Figure 5.** (**a**) Current path for stage 2; (**b**) equivalent of (**a**).

According to Figure 5b, three stage equations can be obtained as

$$\begin{cases} I_{in} = C_{s1}\frac{dv_{ds1}(t)}{dt} + i_{Lr}(t) - C_{s2}\frac{dv_{ds2}(t)}{dt} \\ V_c = v_{ds1}(t) + v_{ds2}(t) \\ v_{ds1}(t) = L_r\frac{di_{Lr}(t)}{dt} + V_o \end{cases} \quad (1)$$

By assuming that two switches are identical, $C_{s1} = C_{s2} = C_s$. Moreover, the initial values of this stage are $i_{Lr}(t_1) = 0$, $v_{ds1}(t_1) = 0$ and $v_{ds2}(t_1) = V_c$. By taking the Laplace transform of Equation (1), the following equations can be attained to be

$$\begin{cases} I_{Lr}(s) = (\frac{1}{s} - \frac{s}{s^2+\frac{1}{2L_rC_s}})I_{in} - (\frac{\frac{1}{L_r}}{s^2+\frac{1}{2L_rC_s}})V_o \\ V_{ds1}(s) = (\frac{1}{s} - \frac{s}{s^2+\frac{1}{2L_rC_s}})V_o + (\frac{\frac{1}{2C_s}}{s^2+\frac{1}{2L_rC_s}})I_{in} \\ V_{ds2}(s) = \frac{V_c}{s} - (\frac{1}{s} - \frac{s}{s^2+\frac{1}{2L_rC_s}})V_o - (\frac{\frac{1}{2C_s}}{s^2+\frac{1}{2L_rC_s}})I_{in} \end{cases} \quad (2)$$

By taking the inverse Laplace transform of Equation (2), the following equations can be attained to be

$$\begin{cases} i_{Lr}(t) = I_{in}[1 - \cos\ \omega_1(t-t_1)] - \frac{V_o}{Z_1}\sin\ \omega_1(t-t_1) \\ v_{ds1}(t) = V_o[1 - \cos\ \omega_1(t-t_1)] + I_{in}Z_1\sin\ \omega_1(t-t_1) \\ v_{ds2}(t) = V_c - V_o[1 - \cos\ \omega_1(t-t_1)] - I_{in}Z_1\sin\ \omega_1(t-t_1) \end{cases} \quad (3)$$

where

$$\omega_1 = \sqrt{\frac{1}{2L_rC_s}} \text{ and } Z_1 = \sqrt{\frac{L_r}{2C_s}} \quad (4)$$

If $\omega_1(t-t_1) \cong 0$, then $\cos\ \omega_1(t-t_1)$ and $\sin\ \omega_1(t-t_1)$ can be close to the following equations:

$$\begin{cases} \cos\ \omega_1(t-t_1) \cong 1 \\ \sin\ \omega_1(t-t_1) \cong \omega_1(t-t_1) \end{cases} \quad (5)$$

Substituting Equation (5) into Equation (3) yields

$$v_{ds2}(t) \cong V_c - I_{in}Z_1\omega_1(t-t_1) \quad (6)$$

According to Equation (6) and $v_{ds}(t_2) = 0$, the corresponding time elapsed $T_2$ is

$$T_2 = t_2 - t_1 = \frac{1}{\omega_1}(\frac{V_c}{I_{in}Z_1}) \quad (7)$$

Stage 3: $(t_2 \le t \le t_3)$

As illustrated in Figures 3 and 6, $S_1$ and $S_2$ are both still OFF. In the previous stage, $v_{ds1}(t_2) = V_c$ and $v_{ds2}(t_2) = 0$. During this stage, $i_{Lr}$ is smaller than $I_{in}$. Hence, $D_{S2}$ is conducted, making $v_{ds1}$ still clamped at $V_c$. At the same time, the voltage across $L_r$ is $V_c - V_o$, causing $i_{Lr}$ to increase linearly. As soon as $S_2$ is conducted, the operation goes to stage 4.

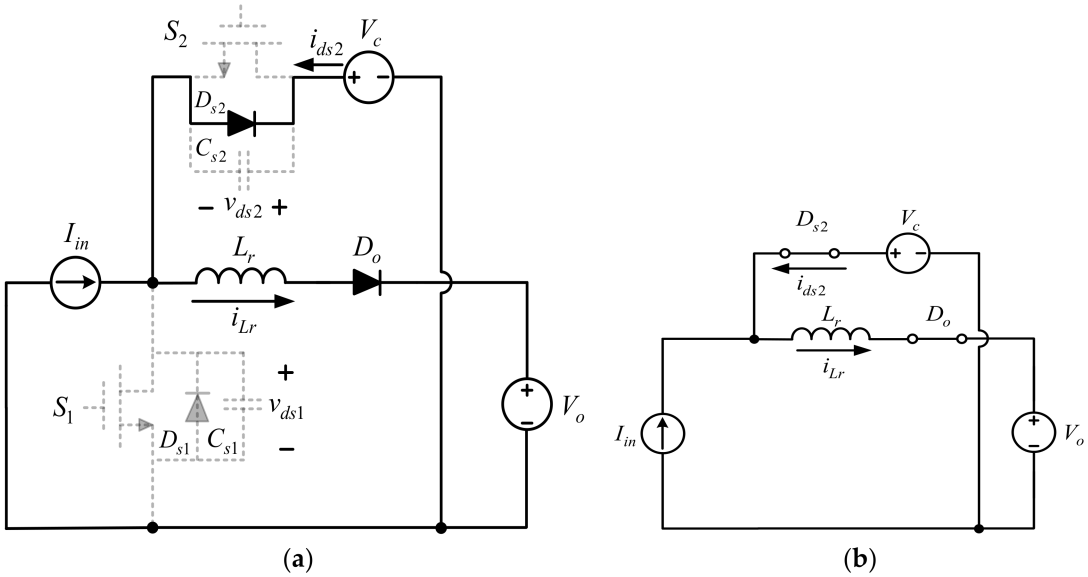


**Figure 6.** (**a**) Current path for stage 3; (**b**) equivalent of (**a**).

According to Figure 6b, one stage equation can be obtained as

$$L_r \frac{di_{Lr}(t)}{dt} = V_c - V_o \tag{8}$$

As the initial value of this stage is $i_{Lr}(t_2) = I_{Lr2}$, solving Equation (8) yields

$$i_{Lr}(t) = \frac{(V_c - V_o)}{L_r}(t - t_2) + I_{Lr2} \tag{9}$$

Since $i_{Lr}(t_3) = I_{Lr3}$, the corresponding time elapsed $T_3$ is

$$T_3 = t_3 - t_2 = \frac{(I_{Lr3} - I_{Lr2})}{V_c - V_o} L_r \tag{10}$$

Stage 4: $(t_3 \leq t \leq t_4)$

As illustrated in Figures 3 and 7, $S_1$ is still OFF, but $S_2$ is conducted. In the previous stage, $v_{ds2}(t_3) = 0$. Therefore, $S_2$ is conducted at $t_3$ with ZVS. As $I_{in}$ is still smaller than $i_{Lr}$, the voltage across $L_r$ is still $V_c - V_o$, causing $L_r$ to still be linearly magnetized. Once $i_{Lr} = I_{in}$, the operation proceeds to stage 5.

One stage equation can be obtained as shown in Figure 7b.

$$L_r \frac{di_{Lr}(t)}{dt} = V_c - V_o \tag{11}$$

As the initial value of this stage is $i_{Lr}(t_3) = I_{Lr3}$, solving Equation (11) yields

$$i_{Lr}(t) = \frac{(V_c - V_o)}{L_r}(t - t_3) + I_{Lr3} \tag{12}$$

Because $i_{Lr}(t_4) = I_{in}$, the corresponding time elapsed $T_4$ is

$$T_4 = t_4 - t_3 = \frac{(I_{in} - I_{Lr3})}{V_c - V_o} L_r \tag{13}$$

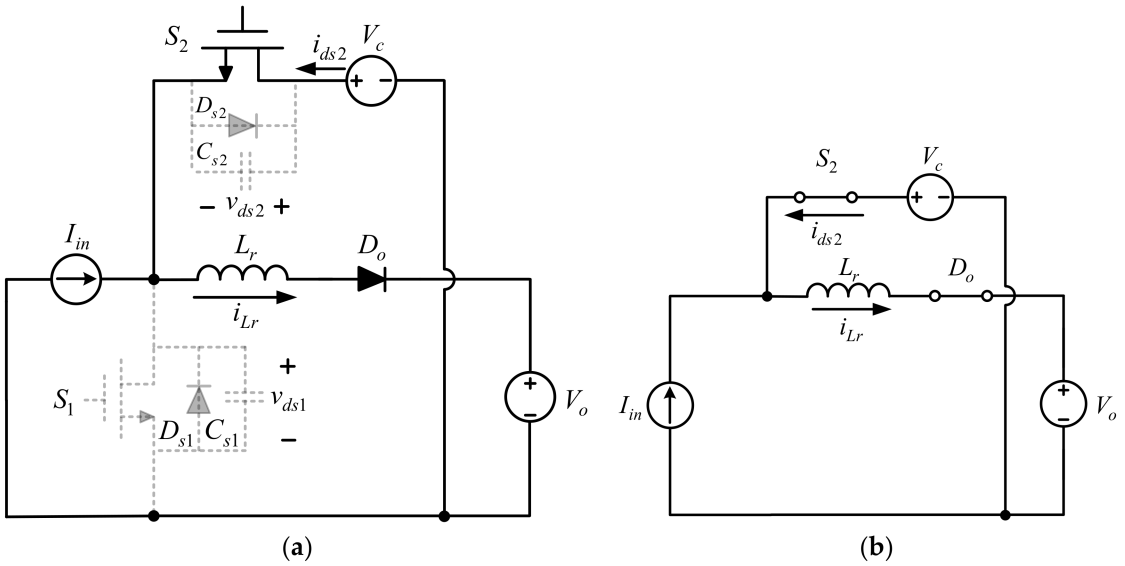


**Figure 7.** (**a**) Current path for stage 4; (**b**) equivalent of (**a**).

Stage 5: $(t_4 \leq t \leq t_5)$

As illustrated in Figures 3 and 8, $S_1$ is still OFF, but $S_2$ is still ON. Hence, the voltage across $S_1$ is clamped at $V_c$. During this stage, $i_{Lr}$ is larger than $I_{in}$, changing $i_{ds2}$ to the positive direction. At the same time, the voltage across $L_r$ is still $V_c - V_o$, causing $L_r$ to still be linearly magnetized. As soon as $S_2$ is cut off, the operation goes to stage 6.

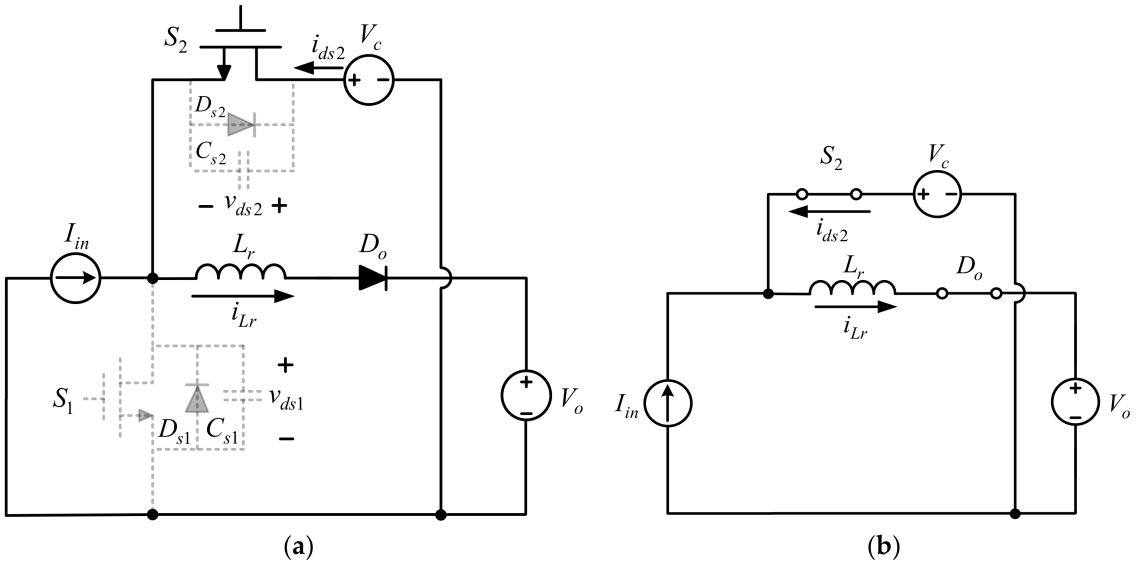


**Figure 8.** (**a**) Current path for stage 5; (**b**) equivalent of (**a**).

One stage equation can be obtained as shown in Figure 8b.

$$L_r \frac{di_{Lr}(t)}{dt} = V_c - V_o \tag{14}$$

As the initial value of this stage is $i_{Lr}(t_4) = I_{in}$, solving Equation (14) yields

$$i_{Lr}(t) = \frac{(V_c - V_o)}{L_r}(t - t_4) + I_{in} \tag{15}$$

Because $i_{Lr}(t_5) = I_{Lr5}$, the corresponding time elapsed $T_5$ is

$$T_5 = t_5 - t_4 = \frac{(I_{Lr5} - I_{in})}{V_c - V_o} L_r \tag{16}$$

Stage 6: $(t_5 \leq t \leq t_6)$

As illustrated in Figures 3 and 9, $S_1$ is still OFF and $S_2$ is cut off. During this stage, $i_{Lr}$ is still large than $I_{in}$, hence $C_{s2}$ is abruptly charged to $V_c$ and $C_{s1}$ is abruptly discharged to zero. At the same time, $L_r$ begins to be demagnetized. The moment $C_{s1}$ is discharged to zero, this stage comes to an end and the next stage begins.

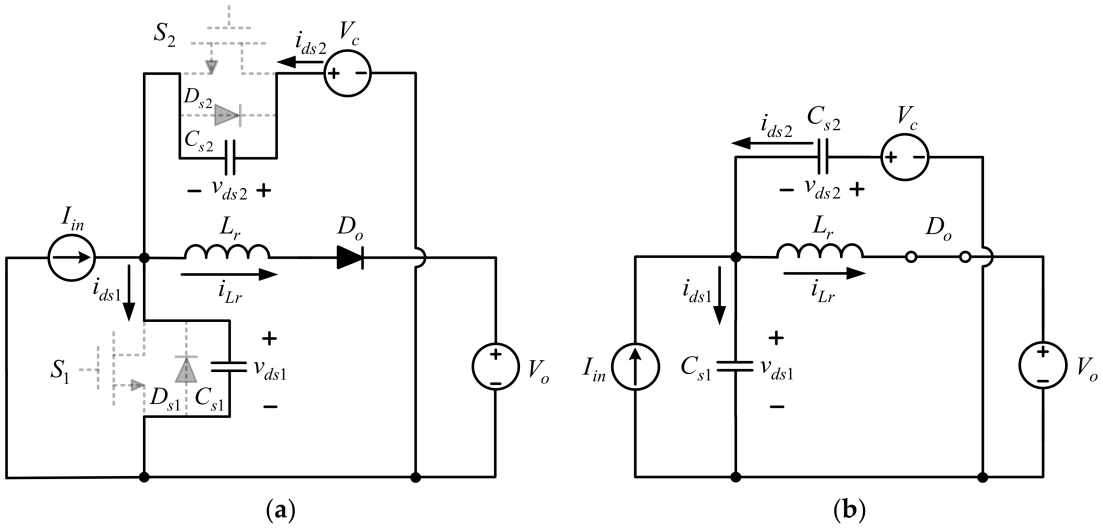


**Figure 9.** (**a**) Current path for stage 6; (**b**) equivalent of (**a**).

Three stage equations can be obtained as shown in Figure 9b.

$$\begin{cases} I_{in} = C_{s1}\frac{dv_{ds1}(t)}{dt} + i_{Lr}(t) - C_{s2}\frac{dv_{ds2}(t)}{dt} \\ V_c = v_{ds1}(t) + v_{ds2}(t) \\ v_{ds1}(t) = L_r\frac{di_{Lr}(t)}{dt} + V_o \end{cases} \tag{17}$$

By assuming two switches are identical, $C_{s1} = C_{s2} = C_s$. Further, the initial values of this stage are $i_{Lr}(t_5) = I_{Lr5}$, $v_{ds1}(t_5) = V_c$ and $v_{ds2}(t_5) = 0$. Based on Equation (4) and by taking the Laplace transform of Equation (17), the following equations can be attained:

$$\begin{cases} I_{Lr}(s) = \frac{I_{in}}{s} - \frac{s}{s^2+\frac{1}{2L_rC_s}}(I_{in} - I_{Lr5}) + \frac{\frac{1}{L_r}}{s^2+\frac{1}{2L_rC_s}}(V_c - V_o) \\ V_{ds1}(s) = \frac{V_o}{s} + \frac{s}{s^2+\frac{1}{2L_rC_s}}(V_c - V_o) + \frac{\frac{1}{2C_s}}{s^2+\frac{1}{2L_rC_s}}(I_{in} - I_{Lr5}) \\ V_{ds2}(s) = \frac{V_c}{s} - \frac{V_o}{s} - \frac{s}{s^2+\frac{1}{2L_rC_s}}(V_c - V_o) - \frac{\frac{1}{2C_s}}{s^2+\frac{1}{2L_rC_s}}(I_{in} - I_{Lr5}) \end{cases} \tag{18}$$

By taking the inverse Laplace transform, the following equations can be attained:

$$\begin{cases} i_{Lr}(t) = I_{in} - (I_{in} - I_{Lr5})\ \cos\ \omega_1(t - t_5) + \frac{(V_c - V_o)}{Z_1}\ \sin\ \omega_1(t - t_5) \\ v_{ds1}(t) = V_o + (V_c - V_o)\ \cos\ \omega_1(t - t_5) + (I_{in} - I_{Lr5})Z_1\ \sin\ \omega_1(t - t_5) \\ v_{ds2}(t) = V_c - V_o - (V_c - V_o)\ \cos\ \omega_1(t - t_5) - (I_{in} - I_{Lr5})Z_1\ \sin\ \omega_1(t - t_5) \end{cases} \tag{19}$$

According to Equations (5) and (19), the equation of $v_{ds2}(t)$ can be simplified to

$$v_{ds2}(t) \cong (I_{Lr5} - I_{in})Z_1\omega_1(t - t_5) \tag{20}$$

According to Equation (20) and $v_{ds2}(t_6) = V_c$, the corresponding time elapsed $T_6$ is

$$T_6 = t_6 - t_5 = \frac{1}{\omega_1}[\frac{V_c}{(I_{Lr5} - I_{in})Z_1}] \tag{21}$$

Stage 7: $(t_6 \leq t \leq t_7)$

As illustrated in Figures 3 and 10, $S_1$ and $S_2$ are still OFF, In the previous stage, $v_{ds1}$ is equal to zero, whereas $v_{ds2}$ is equal to $V_c$. During this stage, $i_{Lr}$ is still larger than $I_{in}$, making $D_{s1}$ conducted, hence $v_{ds2}$ still clamped at $V_c$. At the same time, the voltage across $L_r$ is $-V_o$, causing $L_r$ to be linearly demagnetized. As soon as $S_1$ is conducted, this stage comes to an end and the next stage begins.

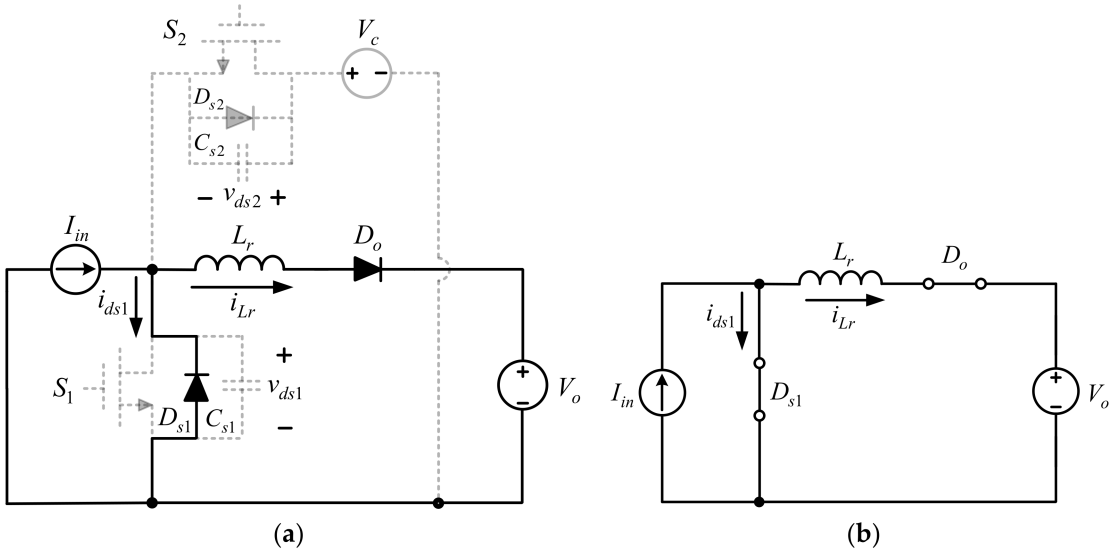


**Figure 10.** (**a**) Current path for stage 7; (**b**) equivalent of (**a**).

According to Figure 10b, one stage equation can be obtained as

$$L_r\frac{di_{Lr}(t)}{dt} = -V_o \tag{22}$$

As the initial value of this stage is $i_{Lr}(t_6) = I_{Lr6}$, solving Equation (22) yields

$$i_{Lr}(t) = I_{Lr6} - \frac{V_o}{L_r}(t - t_6) \tag{23}$$

Because $i_{Lr}(t_7) = I_{Lr7}$, the corresponding time elapsed $T_7$ is

$$T_7 = t_7 - t_6 = \frac{(I_{Lr6} - I_{Lr7})}{V_o}L_r \tag{24}$$

Stage 8: $(t_7 \leq t \leq t_8)$

As illustrated in Figures 3 and 11, $S_1$ is conducted and $S_2$ is still OFF. In the previous stage, $D_{s1}$ is conducted so $S_1$ is switched on with ZVS at $t_7$. As $i_{Lr}$ is still larger than $I_{in}$, the voltage across $L_r$ is still $-V_o$, causing $L_r$ to be still linearly demagnetized. As $i_{Lr} = I_{in}$, this stage ends and the next stage starts.

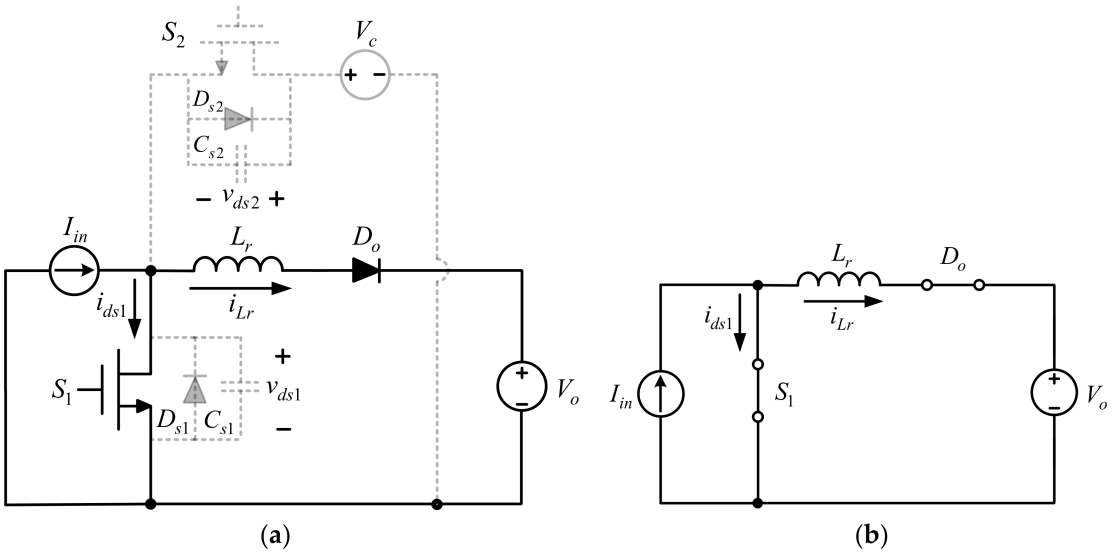


**Figure 11.** (**a**) Current path for stage 8; (**b**) equivalent of (**a**).

According to Figure 11b, one stage equation can be obtained as

$$L_r \frac{di_{Lr}(t)}{dt} = -V_o \tag{25}$$

As the initial value of this stage is $i_{Lr}(t_7) = I_{Lr7}$, solving Equation (25) yields

$$i_{Lr}(t) = i_{Lr7} - \frac{V_o}{L_r}(t - t_7) \tag{26}$$

Because $i_{Lr}(t_8) = I_{in}$, the corresponding time elapsed $T_8$ is

$$T_8 = t_8 - t_7 = \frac{(I_{Lr7} - I_{in})}{V_o} L_r \tag{27}$$

Stage 9: ($t_8 \leq t \leq t_0 + T_s$)

As illustrated in Figures 3 and 12, $S_1$ is still ON but $S_2$ is still OFF. Hence, $v_{ds2}$ is clamped at $V_c$. During this stage, $i_{Lr}$ is smaller than $I_{in}$, changing $i_{ds1}$ to the positive direction. At the same time, the voltage across $L_r$ is $-V_o$, causing $L_r$ to still be linearly demagnetized. From Figure 3, it can be seen that, as $i_{Lr} = 0$, the output diode $D_o$ is cut off before the turn-off time point of $v_{gs1}$, meaning that $D_o$ has ZCS turn-off. Once $i_{Lr} = 0$, this stage ends with the next cycle repeated.

According to Figure 12b, one stage equation can be obtained as

$$L_r \frac{di_{Lr}(t)}{dt} = -V_o \tag{28}$$

As the initial value of this stage is $i_{Lr}(t_8) = I_{in}$, solving Equation (28) yields

$$i_{Lr}(t) = I_{in} - \frac{V_o}{L_r}(t - t_8) \tag{29}$$

Because $i_{Lr}(t_0 + T_s) = 0$, the corresponding time elapsed $T_9$ is

$$T_9 = t_0 - t_8 = \frac{I_{in}}{V_o} L_r \tag{30}$$

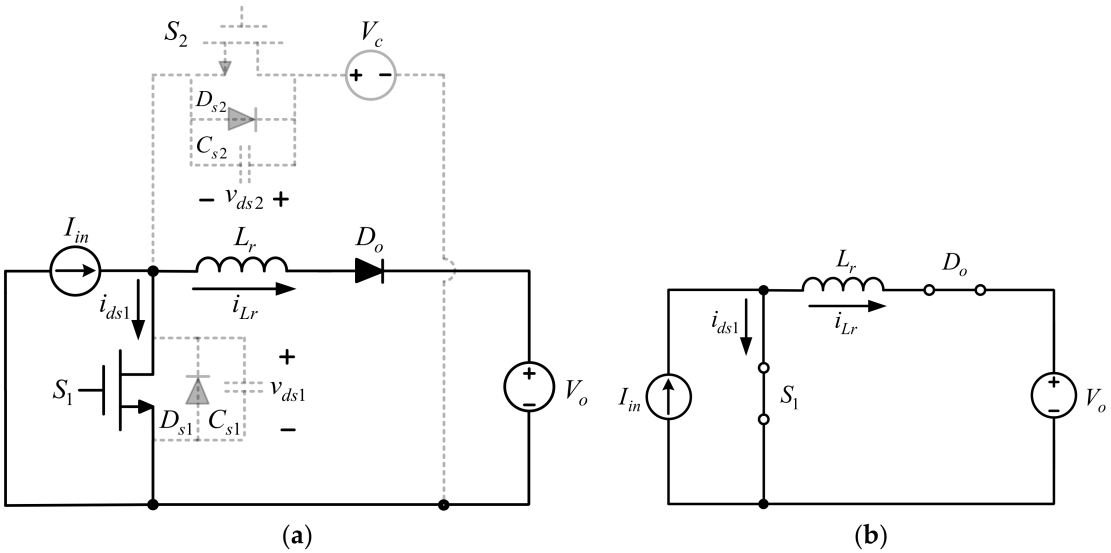


**Figure 12.** (**a**) Current path for stage 9; (**b**) equivalent of (**a**).

If $T_8$ plus $T_9$, which is about $T_9$, is smaller than $t_{on}$, i.e., $DT_s$, the resonant inductor $L_r$ works in DCM, meaning that there is no reverse recovery current during the turn-off period of $D_o$. Because $v_{gs1}$ and $v_{gs2}$ have two blanking times between them per cycle, if $T_9$ is larger than $t_{on}$, then at the instant when $S_1$ is cut off, but $S_2$ is still OFF, $i_{Lr}$ will flow through $D_{s1}$. Once $S_2$ is turned on, a large reverse recovery current will flow through $S_2$ owing to a reverse voltage of $V_c$ across $D_{s1}$. Accordingly, $S_2$ may be destroyed as a result of this current spike or $S_1$ is turned on again, causing shoot-through between $S_1$ and $S_2$.

Table 1 is used to summarize soft switching types in the proposed converter.

**Table 1.** Soft switching type. ZVS, zero voltage switching; ZCS, zero current switching.

| Interval | Stage | Type |
|---|---|---|
| $t_3 \leq t \leq t_4$ | 4 | $S_2$ ZVS turn-on |
| $t_7 \leq t \leq t_8$ | 8 | $S_1$ ZVS turn-on |
| $t_8 \leq t \leq t_0 + T_s$ | 9 | $D_o$ ZCS turn-off |

2.2.2. Voltage Gain

By applying the voltage-second balance to $L_{in}$, we can obtain

$$\frac{1}{T_s}\int_t^{t+T_s} v_{Lin}(\tau)d\tau = V_{in}(D+\alpha) + (V_{in} - V_c)(1 - D - \alpha) = 0 \tag{31}$$

By rearranging Equation (31), we can obtain

$$\frac{V_c}{V_{in}} = \frac{1}{1 - D - \alpha} \tag{32}$$

where

$$\alpha = \frac{T_6 + T_7}{T_s} \tag{33}$$

By applying the voltage-second balance to $L_r$, we can obtain

$$\begin{aligned} &\tfrac{1}{T_s}\textstyle\int_t^{t+T_s} v_{Lr}(\tau)d\tau \\ &= (V_c - V_o)(1 - D - \alpha) + (-V_o)(\alpha + \beta) = 0 \end{aligned} \tag{34}$$

By rearranging Equation (34), we can obtain

$$\frac{V_o}{V_c} = \frac{1 - D - \alpha}{1 - D + \beta} \tag{35}$$

where

$$\beta = \frac{T_8 + T_9}{T_s} \tag{36}$$

Substituting Equation (35) into Equation (32) yields

$$\frac{V_o}{V_{in}} = \frac{1}{1 - D + \beta} \tag{37}$$

It can be seen from Equation (35) that the active clamp voltage $V_c$ is larger than the output voltage $V_o$, whereas it can also be seen from Equation (37) that this voltage gain is smaller than that of the conventional boost converter in CCM.

## 3. Design Considerations

Table 2 shows the system specifications, whereas Table 3 shows the component specifications.

**Table 2.** System specifications. CCM, continuous conduction mode.

| Scheme 24. | Specifications |
|---|---|
| Operation Mode | CCM |
| Input Voltage ($V_{in}$) | 24 V |
| Output Voltage ($V_o$) | 42 V |
| Ideal Duty Cycle ($D$) | 0.43 |
| Switching Frequency ($f_s$) | 100 kHz |
| Output Rated Power ($P_{o,rated}$)/Current ($I_{o,rated}$) | 100 W/2.38 A |
| Output Minimum Power ($P_{o,min}$)/Current ($I_{o,min}$) | 10 W/0.238 A |

**Table 3.** Component Specifications.

| Components | Specifications |
|---|---|
| Input Inductance ($L_{in}$) | 150 µH |
| Resonant Inductance ($L_r$) | 10 µH |
| Output Capacitance ($C_o$) | 470 µF |
| Clamp Capacitance ($C_c$) | 2.2 µF |
| Power Switches ($S_1$ and $S_2$) | IRF540 |
| Output Diode ($D_o$) | STPS20120C |
| Field Programmable Gate Array (FPGA) | EP2C20F484C8 |

### 3.1. Design of Input Capacitance $C_o$

As for output capacitor design, Equation (38) is used on condition that the maximum output voltage ripple $\Delta v_{o,max}$ is equal to 0.1% of the output voltage $V_o$, the value of $R$ is 17.6 Ω, $T_s$ is 10 µs, $D$ = 0.43, and $V_o$ = 42 V. After some calculations, the value of $C_o$ is larger than 244 µF. Eventually, a 470 µF capacitor is chosen, because the value of the electrolytic capacitor will be decreased if the switching frequency is increased.

$$C_{o,min} = \frac{V_o D T_s}{\Delta v_{o,max} R} \tag{38}$$

### 3.2. Design of Input Inductance $L_{in}$

Because the converter operates in the CCM for any load, the minimum value of $L_{in}$, called $L_{in,min}$, can be represented by

$$L_{in,min} = \frac{R_{max} D(1-D)^2 T_s}{2} \tag{39}$$

where $R_{max}$ = 176 Ω, $D$ = 0.43, and $T_s$ = 10 μs.

Based on Equation (39), $L_{in,min}$ = 123 μH after some calculations and, eventually, the value of $L_{in}$ is chosen to be 150 μH by considering the inductance reduction owing to the temperature and load. After this, a T175-18 core, manufactured by Micrometals, Inc. (Anaheim, CA, USA) is utilized, which has an inductance coefficient $A_{L1}$ of 82 nH/N$^2$, and hence the number of turns, called $N_{in}$, is

$$N_{in} = \sqrt{\frac{L_{in} \times 1000}{A_{L1}}} = \sqrt{\frac{150 \times 1000}{82}} = 42.76 \tag{40}$$

Eventually, based on Equation (40), the value of $N_{in}$ is chosen to be 43.

### 3.3. Design of Resonant Capacitance $C_s$

According to stage 2 in Section 2 with $C_{s1} = C_{s2} = C_s$, from Equation (7), we can obtain the following:

$$V_c = \frac{I_{in} \times T_2}{2C_s} \tag{41}$$

From Equation (32), we can get the relationship between $V_{in}$ and $V_c$, with α being positive and smaller than 1, as shown in Equation (42):

$$V_c = \frac{V_{in}}{1 - D - \alpha} > V_o \tag{42}$$

During stage 2, $v_{ds1}$ rises from zero to $V_c$ and $v_{ds2}$ falls from $V_c$ to zero. Based on the IRF540 datasheet and its characteristic curves of rising time $t_r$ and falling time $t_f$ versus drain current $I_{ds}$, we can know that the value of $T_2$ is about 0.02 μs. Hence, from Equations (41) and (42), we can attain the inequation of the resonance capacitance $C_s$ to be

$$C_s < \frac{4.21 \times 0.02\ \mu s}{42 \times 2} = 1 nF \tag{43}$$

As the resonant capacitance $C_s$ is equal to the parasitic capacitance of the power switch, two IRF540 MOSFETs with typical output capacitance of 125 pF are chosen for $S_1$ and $S_2$ to meet the requirements of Equation (43).

### 3.4. Design of Resonant Inductance $L_r$

After the resonant capacitance $C_s$ is determined, the design of the resonant inductance $L_r$ will follow. As the resonant radian frequency $\omega_1$ is desired not to affect the operation behavior of the converter, the value of $\omega_1$ ten times larger than the value of the switching radian frequency $\omega_s$, namely, $\omega_1 > 2\pi \times 10^6$ rad/ sec. Therefore, based on Equations (43) and (44), the inequality of $L_r$ can be obtained to be

$$L_r < \frac{1}{2 \times (2\pi \times 10^6)^2 \times C_s} = \frac{1}{2 \times (2\pi \times 10^6)^2 \times 10^{-9}} = 12.6\ \mu H \tag{44}$$

Accordingly, the value of $L_r$ is chosen to be 10 μH. After this, a T175-18 core, manufactured by ARNOLD Co., is adopted, which has an inductance coefficient $A_{L1}$ of 75 nH/N$^2$, and hence the number of turns, called $N_r$, is

$$N_r = \sqrt{\frac{L_r \times 1000}{A_{L2}}} = \sqrt{\frac{10 \times 1000}{75}} = 11.55 \tag{45}$$

Finally, based on Equation (45), the value of $N_r$ is chosen to be 11.

### *3.5. Design of Active Clamp Capacitor $C_c$*

Regarding the design of the active clamp capacitor $C_c$, it can be designed based on the required voltage ripple $\Delta v_c$. From stages 2, 3, 4, 5, and 6 and Figure 3, it can be seen that $C_c$ has the behavior of slight charge and discharge. Therefore, the product of $C_c$ and $\Delta v_c$ can be expressed as

$$C_c \Delta v_c = \Delta Q_c = \frac{1}{2}(i_{ds2,max})(T_5 + T_6) \tag{46}$$

where $T_5$ and $T_6$ are the times elapsed for stages 5 and 6, respectively.

Because individual switch parasitic capacitors in stages 2 and 6 have charge and discharge, the corresponding times elapsed are so short. Therefore, if two switches are identical, then

$$T_6 \cong T_2 = 0.02\ \mu \tag{47}$$

Accordingly, based on Equation (16), $T_5$ plus $T_6$ can be represented by

$$T_5 + T_6 = \frac{(I_{Lr5} - I_{in})}{V_c - V_o} L_r + 0.02\ \mu \tag{48}$$

In order to find the value of $C_c$, the currents $i_{ds2,max}$ and $I_{Lr5}$ should be figured out first. From stage 5 and Figure 8, the value of $i_{ds1,max}$ can be obtained to be

$$i_{ds2}(t_5) = i_{ds2,max} = i_{Lr}(t_5) - I_{in} = I_{Lr5} - I_{in} \tag{49}$$

From Equation (49), the value of $I_{Lr5}$ should be figured out first, via stages 2 and 6 in Section 2.2.1. Based on Equations (7), (21) and (47), the following equation can be obtained to be

$$\frac{1}{\omega_1}[\frac{V_c}{(I_{Lr5} - I_{in})Z_1}] \cong \frac{1}{\omega_1}(\frac{V_c}{I_{in}Z_1}) \tag{50}$$

Rearranging Equation (50) yields

$$I_{Lr5} \cong 2I_{in} \tag{51}$$

Finally, substituting Equation (51) into Equation (49) yields

$$i_{ds2,max} \cong 2I_{in} - I_{in} = I_{in} \tag{52}$$

As $I_{in} = I_{o,rated}/(1\text{-}D)$, $I_{in}$ can be obtained to be 4.165A from Table 2, if the voltage ripple $\Delta v_c$ has 5% of $V_c$, then, substituting Equations (48), (51), and (52) into Equation (46), the value of $C_c$ can be expressed to be

$$C_c = \frac{86.94\ \mu + 0.04\ \mu V_c}{0.05\ V_c(V_c - 42)} \tag{53}$$

To solve the value of $C_c$, the value of $V_c$ should be figured out first. From Figure 3, the following equation can be obtained:

$$\sum_{n=2}^{7} T_n = (1 - D)T_s \tag{54}$$

Sequentially, from stage 2 in Section 2.2.1, the following equation can be obtained:

$$I_{in} = i_{ds1}(t_2) + i_{Lr}(t_2) - i_{ds2}(t_2) \tag{55}$$

From Section 2.2.1, it can be seen that $i_{ds1}(t_2) = 0$ can be found and $i_{Lr}(t_2) \cong 0.22$ A can be found based on Equation (3) and $T_2 \cong 0.02$ µs. Substituting $i_{ds1}(t_2) = 0$ and $i_{Lr}(t_2) \cong 0.22$ A into Equation (55) yields

$$i_{ds2}(t_2) \cong -I_{in} \tag{56}$$

In addition, from stages 3 to 5, the voltage across $L_r$ is $V_c - V_o$, thereby causing $L_r$ to be linearly magnetized with $i_{Lr}(t) = I_{in} + i_{ds2}(t)$, hence $i_{ds2}(t)$ has the same slope from stages 3 to 5. Accordingly, based on the ampere-second balance, the following equation can be obtained:

$$T_2 + T_3 + T_4 \cong T_5 + T_6 \tag{57}$$

From Equations (33) and (47), the following equation can be obtained:

$$T_7 = \alpha T_s - 0.02\ \mu \tag{58}$$

Based on Equations (48), (54), (57), and (58), the following equation can be obtained:

$$\sum_{n=2}^{7} T_n = 2 \times \left(\frac{I_{Lr5} - I_{in}}{V_c - V_o} L_r + 0.02\ \mu\right) + 10\ \mu\alpha - 0.02\ \mu = (1 - D)T_s \tag{59}$$

Based on Table 2 and the obtained values, Equation (59) can be rewritten to be

$$210\ \mu\alpha^2 - 161.08\ \mu\alpha + 23.72\ \mu = 0 \tag{60}$$

Solving Equation (60) yields

$$\alpha \cong 0.19,\ 0.568 \tag{61}$$

If $\alpha = 0.568$, this means that the auxiliary switch has only turn-on time of 0.02 µs. By considering the rising and falling times, $\alpha$ is chosen to be 0.19. Substituting $\alpha$ into Equation (32) yields

$$V_c = \frac{24}{1 - 0.43 - 0.19} = 63.2\ \text{V} \tag{62}$$

Substituting Equation (62) into Equation (53) yields

$$C_c = \frac{86.94\ \mu + 0.04\ \mu \times 63.2}{0.05 \times 63.2(63.2 - 42)} \tag{63}$$

Solving Equation (63) yields $C_s \cong 1.33$ µF. Eventually, the value of $C_s$ is selected as 2.2 µF.

## 4. Digital Control Flow Chart

As shown in Figure 13a, there are five modules in the digital control strategy, including output voltage sampling, named V_sample; input current sampling, named I_sample; look-up table; digital controller; and digital pulse width modulation generator, named DPWM.

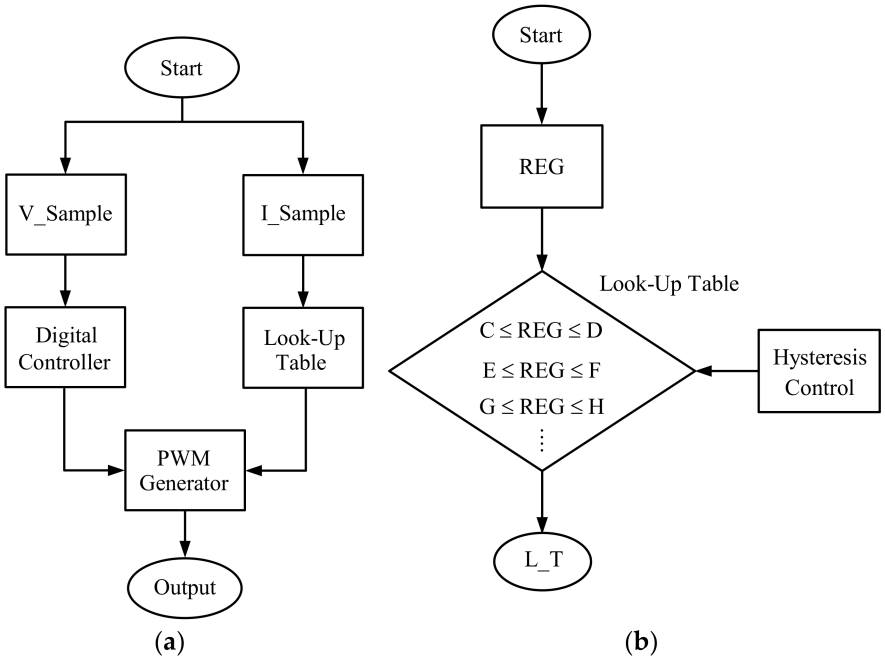


**Figure 13.** (**a**) System operation flow chart; (**b**) look-up table operation flow chart. PWM, pulse width modulation.

### *4.1. System Operation*

In Figure 13a, the output voltage and the input current are sensed by the V_sample module and the I_sample module, respectively. The sensed output voltage is sent to the digital controller and then to the DPWM generator to create a suitable gate driving signal for the switch $S_1$, so as to keep the output voltage constant at a desired value. The sensed current is sent to the look-up table to generate a suitable gate driving signal for the switch $S_2$, so that the cut-off time point of the auxiliary switch $S_2$ can be determined.

### *4.2. Auto Tuning of the Last Blanking Time of $S_2$*

From Section 2, we can see that as the auxiliary switch $S_2$ is cut off, the resonant inductor $L_r$ begins to be demagnetized, and the demagnetization path will pass through $D_o$, leading to the power dissipation in $D_o$. Accordingly, cutting off $S_2$ early reduces the required time flowing through $D_o$, hence the power dissipation in $D_o$ will be decreased, increasing the overall efficiency. Therefore, a lookup table is built up with the relationship between the cut-off time point of $S_2$ and load current $I_o$. However, it is noted that, as for the auto tuning of the cut-off time point for $S_2$, the resonant current $i_{Lr}$ should be larger than the input current $I_{in}$ before the main switch $S_1$ is switched on so as to make sure that $S_1$ is switched on with ZVS. In the following, how to construct this lookup table is mentioned below.

Step 1

Under an open-loop test with ten points from light to rated load, the maximum efficiency for each sensed input current is obtained by manually tuning the cut-off time point of the auxiliary switch $S_2$. This sensed input current is digitalized and then used to generate one interval value in a look-up table.

Step 2

For each point, the corresponding cut-off time point of $S_2$ under the maximum efficiency is recorded.

Step 3

A lookup table with cut-off time point of $S_2$ versus interval value created from the input current is established as shown in Figure 13b. After this, as an actual input current is sensed and digitalized; this value will be stored in the register REG and then compared with interval values in the lookup-up table to obtain the required cut-off time point of $S_2$, called L_T. The corresponding gate driving signal for $S_2$ is obtained as illustrated in Figure 14. Accordingly, the proposed converter will do a good performance on efficiency under different input current levels. It is noted that the hysteresis band is applied to the exchange of two cut-off time points to avoid oscillation.

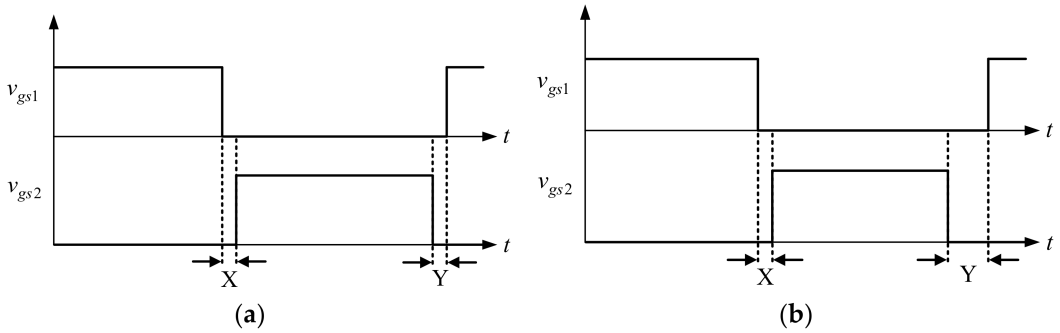


**Figure 14.** Auto-tuning technique with X and Y called the first blanking time and the second blanking time, respectively: (**a**) with X = Y ; (**b**) with X ≠ Y.

It is noted that the proposed auto-tuning technique is used in the steady state. First, the input current $I_{in}$ is sampled at a time point within the turn-on time $t_{on}$ of $v_{gs1}$. After this, based on the lookup table, the corresponding cut-off time point of $v_{gs2}$ for the auxiliary switch $S_2$ will be determined, which will be used in the next cycle of $v_{gs2}$. As to $v_{gs1}$ for the main switch $S_1$, it is almost not changed because the duty cycle of $v_{gs1}$ is generated from the controller, hence the system stability is almost not affected.

## 5. Results and Discussion

At a rated load, Figure 15 shows the gate driving signals for $S_1$ and $S_2$, called $v_{gs1}$ and $v_{gs2}$, respectively. Figure 16 shows the gate driving signal for $S_1$, called $v_{gs1}$; the voltage on $S_1$, called $v_{ds1}$; and the current in $S_1$, called $i_{ds1}$. Figure 17 shows the gate driving signal for $S_2$, called $v_{gs2}$; the voltage on $S_2$, called $v_{ds2}$; and the current in $S_2$, called $i_{ds2}$. Figure 18 shows the voltage on $C_c$, called $v_c$, and the current in $L_r$, called $i_{Lr}$. Figure 19 shows the voltage on $D_o$, called $v_{Do}$, and the current in $L_r$, called $i_{Lr}$. Figure 20 shows the efficiency comparison.

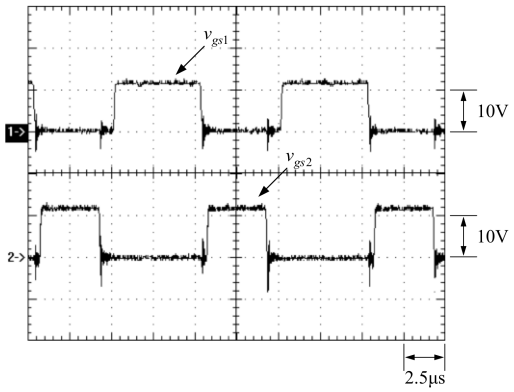


**Figure 15.** Experimental waveforms: (1) $v_{gs1}$; (2) $v_{gs2}$.

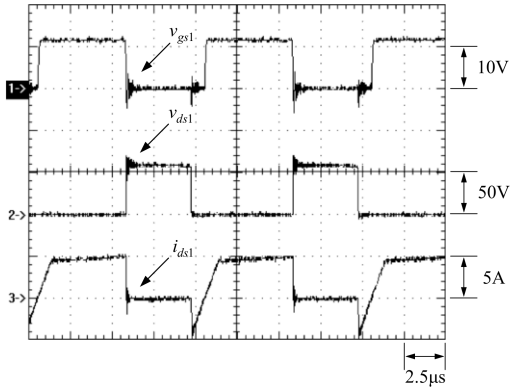


**Figure 16.** Experimental waveforms: (1) $v_{gs1}$; (2) $v_{ds1}$; (3) $i_{ds1}$.

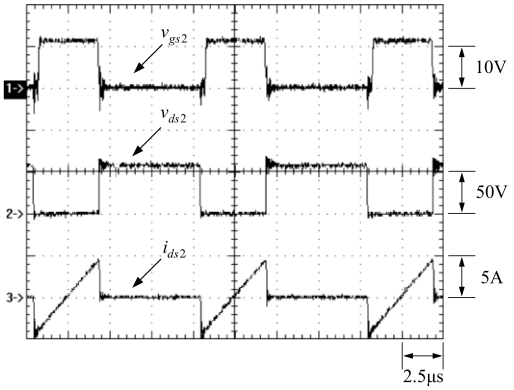


**Figure 17.** Experimental waveforms: (1) $v_{gs2}$; (2) $v_{ds2}$; (3) $i_{ds2}$.

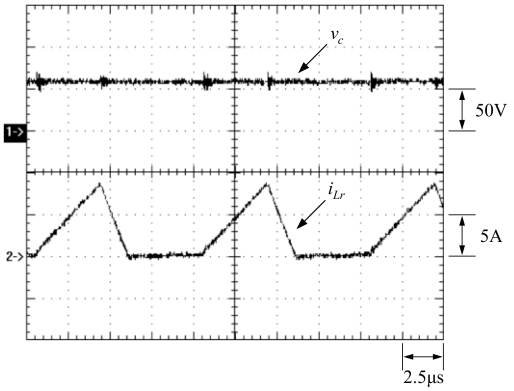


**Figure 18.** Experimental waveforms: (1) $v_c$; (2) $i_{Lr}$.

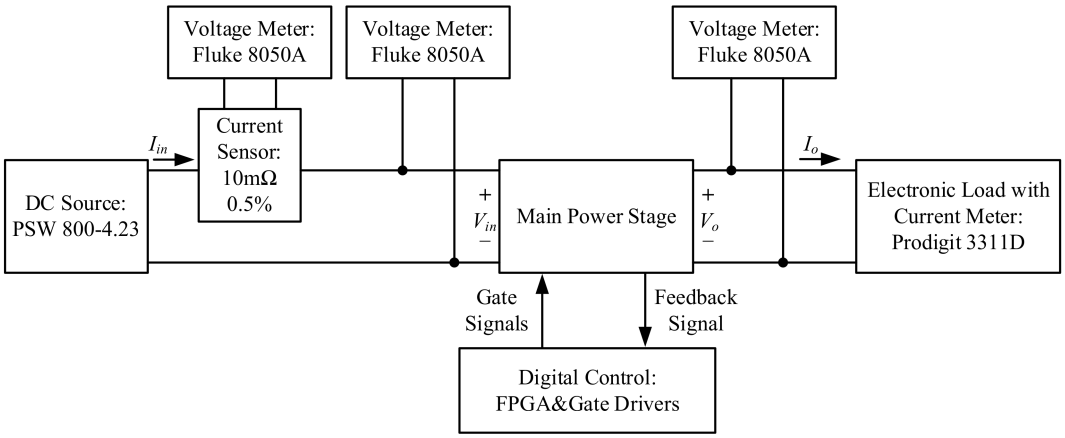


**Figure 19.** Efficiency test bench. (DC: direct current; FPGA: field programmable gate array).

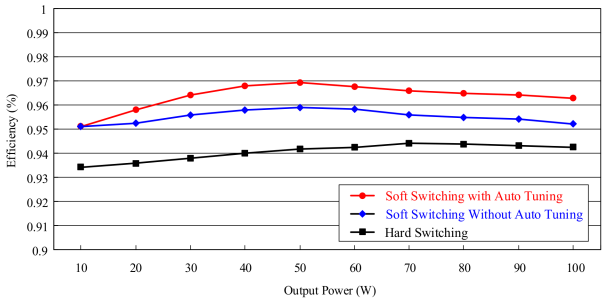


**Figure 20.** Efficiency comparison.

From Figure 15, it can be seen that $v_{gs1}$ and $v_{gs2}$ are complementary to each other. From Figure 16, before $S_1$ is turned on, $i_{ds1}$ flows in the opposite direction, causing $C_{s1}$ to be discharged to zero, making $D_{s1}$ forward biased. At this moment, $S_1$ is switched on with ZVS. From Figure 17, before $S_2$ is turned on, $i_{ds2}$ flows in the opposite direction, causing $C_{s2}$ to be discharged to zero, making $D_{s2}$ forward biased. At this moment, $S_2$ is switched on with ZVS. From Figure 18, it can be seen that $v_c$ is almost kept constant at about 60 V, close to Equation (62). In addition, according to Equation (30), the ideal value of $T_9$ can be figured out to be

$$T_9 = \frac{Iin}{V_o} L_r = \frac{I_{o,rated} L_r}{V_o(1-D)} = \frac{2.38 \times 1\ \mu}{42(1-0.43)} = 1\ \mu s \tag{64}$$

From Equation (64), the ideal value of $T_9$ is smaller than the ideal value of $t_{on}$ of $v_{gs1}$, i.e., 4.3 µs. Moreover, from Figure 18, the calculated value of $T_9$ is 1.36 µs, which is located between 1 µs and 4.3 µs. Therefore, we can confirm that the output diode has ZCS turn-off.

In the following, an efficiency test bench will be described as shown in Figure 19. First of all, the input current $I_{in}$ is attained by measuring the voltage on one current-sensing resistor according to one digital meter. Afterwards, the input voltage $V_{in}$ is also attained by another digital meter. Therefore, the input power can be attained. As to the output power, the output current $I_o$ is read from one electronic load and the output voltage $V_o$ is also attained by the other digital meter. Thus, the output power can be attained. Eventually, the required efficiency can be attained. In Figure 20, there are three cases used for efficiency comparison. Case 1 is under soft switching with auto tuning of the turn-off time point of the auxiliary switch. Case 2 is only under soft switching without auto tuning of the turn-off time point of the auxiliary switch. Case 3 is only under the hard switching without auto tuning of the turn-off time point of the auxiliary switch. Therefore, at 10% load, all three have the same the second blanking time, leading to the efficiencies for cases 1 and 2 being the same. As the load is increased, only the second blanking time in case 1 is changed. From

Figure 20, it can be seen that the proposed soft switching with auto tuning of the cut-off time point of the auxiliary switch has the best performance in efficiency among them.

## 6. Conclusions and Future Work

The traditional boost converter, having an active clamp circuit along with the resonant inductor, is presented herein. Both the main switch and the auxiliary switch can be turned on with ZVS and the output diode can be turned off with ZCS. In addition, as the active clamp circuit is utilized, the voltage spike on the main switch can be suppressed to some extent, whereas because this structure, although the input inductor is designed in CCM, the output diode can operate with ZCS turn-off, leading to the resonant inductor operating in DCM, hence there is no reverse recovery current during the turn-off period of the output diode. Unlike the existing soft switching circuits, in order to improve the overall efficiency further, one look-up table is employed to adjust the cut-off time point of the auxiliary switch so that the current flowing through the output diode is reduced. By doing so, the maximum efficiency is 96.9%. In this paper, the cut-off time point of the auxiliary switch is adjusted only in the steady state. In the future, adjusting the cut-off time point for the auxiliary switch in the transient will be studied. In addition, the MOSFETs and Schottky diode used are all Si-based. For high switching frequency applications, SiC- or GaN-based semiconductors can be more attractive than Si-based ones. This will also be studied.

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## Abbreviations

| | |
|---|---|
| $S_1$ | Main switch |
| $S_2$ | Auxiliary switch |
| $L_{in}$ | Input inductor |
| $L_r$ | Resonant inductor |
| $C_o$ | Output capacitor |
| $C_c$ | Active clamp capacitor |
| $C_{s1}$ | Parasitic capacitor of $S_1$ |
| $C_{s2}$ | Parasitic capacitor of $S_2$ |
| $D_o$ | Output diode |
| $D_{s1}$ | Body diode of $S_1$ |
| $D_{s2}$ | Body diode of $S_2$ |
| $R$ | Output resistor |
| $R_{max}$ | Maximum output resistance |
| $\omega_1$ | Resonant radian frequency |
| $\omega_s$ | Switching radian frequency |
| $Z_1$ | Characteristic impedance |

| | |
|---|---|
| $T_s$ | Switching period |
| $f_s$ | Switching frequency |
| $D$ | Duty cycle |
| $V_{in}$ | Input dc voltage |
| $V_o$ | Output dc voltage |
| $V_c$ | Active clamp dc voltage |
| $\Delta v_{o,max}$ | Maximum output voltage ripple |
| $\Delta v_c$ | Active clamp voltage ripple |
| $v_c$ | Active clamp voltage |
| $v_{gs1}$ | Gate driving signal for $S_1$ |
| $v_{gs2}$ | Gate driving signal for $S_2$ |
| $v_{ds1}$ | Voltage across $S_1$ |
| $v_{ds2}$ | Voltage across $S_2$ |
| $v_{Do}$ | Voltage across $D_o$ |
| $I_{in}$ | Input dc current |
| $I_{in,rated}$ | Rated input dc current |
| $I_o$ | Output dc current |
| $I_{o,rated}$ | Rated output dc current |
| $I_{o,min}$ | Minimum output dc current |
| $i_{ds1}$ | Current flowing through $S_1$ |
| $i_{ds2}$ | Current flowing through $S_2$ |
| $i_{Lr}$ | Current flowing through $L_r$ |
| $P_{o,rated}$ | Rated output power |
| $P_{o,min}$ | Minimum output power |
| $L\_T$ | Auto-tuning of the cut-off time point of $S_2$ |
| X | Front edge blanking time |
| Y | Back edge blanking time |
| $\alpha$ | $T_6$ plus $T_7$ divided by $T_s$ |
| $\beta$ | $T_8$ plus $T_9$ divided by $T_s$ |
| $t_0$ to $t_0 + T_s$ | Time points used in Figure 3 |
| $T_2$ to $T_9$ | Elapsed times for operating stages |
| $I_{Lr2}$ to $I_{Lr7}$ | Currents in Lr for time points in Figure 3 |
| $i_{ds2,max}$ | Maximum current flowing through $S_2$ |
| $N_{in}$ | Number of turns for $L_{in}$ |
| $N_r$ | Number of turns for $L_r$ |
| $A_{L1}$ | Inductor coefficient for $L_{in}$ |
| $A_{L2}$ | Inductor coefficient for $L_r$ |
| $L_{in,min}$ | Minimum input inductance |
| $\Delta Q_c$ | Net charge in $C_c$ |

## References


1. Jain, P.; Soin, H.; Cardella, M. Constant frequency resonant DC/DC converters with zero switching losses. *IEEE Trans. Aerosp. Electron. Syst.* **1994**, *30*, 534–644. [CrossRef]
2. Wang, C.-M. New family of zero-current-switching PWM converters using a new zero-current-switching PWM auxiliary circuit. *IEEE Trans. Ind. Electron.* **2006**, *53*, 768–777. [CrossRef]
3. Chen, W.; Ruan, X.; Chen, Q.; Ge, J. Zero-coltage-switching PWM full-bridge converter employing auxiliary transformer to reset the clamping diode current. *IEEE Trans. Power Electron.* **2010**, *25*, 1149–1162. [CrossRef]
4. Tseng, C.; Chen, C. A novel ZVT PWM cuk power-factor corrector. *IEEE Trans. Ind. Electron.* **1999**, *46*, 780–787. [CrossRef]
5. Park, N.; Hyun, D. N Interleaved boost converter with a novel ZVT cell using a single resonant inductor for high power applications. In Proceedings of the Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting, Tampa, FL, USA, 8–12 October 2006; pp. 2157–2161.
6. Li, W.; Wu, J.; Xie, R.; He, X. A non-isolated interleaved ZVT boost converter with high step-up conversion derived from its isolated counterpart. In Proceedings of the 2007 European Conference on Power Electronics and Applications, Aalborg, Denmark, 2–5 September 2007; pp. 1–8. [CrossRef]
7. Yao, G.; Ma, M.; Deng, Y.; Li, W.; He, X. An improved ZVT PWM three level boost converter for power factor preregulator. In Proceedings of the 2007 IEEE Power Electronics Specialists Conference, Orlando, FL, USA, 17–21 June 2007; pp. 768–772. [CrossRef]

8. Chen, Z.; Ji, B.; Ji, F.; Shi, L. Analysis and design considerations of an improved ZVS full-bridge DC-DC converter. In Proceedings of the 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Palm Springs, CA, USA, 21–25 February 2010; pp. 1471–1476. [CrossRef]
9. Bodur, H.; Bakan, A.F. A new ZVT-ZCT-PWM DC-DC converter. *IEEE Trans. Power Electron.* **2004**, *19*, 676–684. [CrossRef]
10. Lin, J.; Hsieh, J.; Yeh, I. A novel ZCZVT soft-switching single-stage high power factor correction. In Proceedings of the 2004 IEEE Asia-Pacific Conference on Circuits and Systems, Tainan, Taiwan, 6–9 December 2004; pp. 2016–2021.
11. Hwu, K.; Shieh, J.; Jiang, W. Interleaved boost converter with ZVT-ZCT for main switches and ZCS for auxiliary switch. *Appl. Sci.* **2020**, *10*, 2033. [CrossRef]
12. Lin, B.; Chiang, H.; Huang, C.; Wang, D. Analysis, design and implementation of an active clamp forward converter with synchronous rectifier. In Proceedings of the 2005 IEEE International Conference on Computers Communications, Control and Power Engineering (TENCON), Melbourne, Australia, 21–24 November 2005; pp. 1427–1432. [CrossRef]
13. Acik, A.; Cadirci, I. Active clamped ZVS forward converter with soft-switched synchronous rectifier for high efficiency, low output voltage applications. *IEEE Electron. Power Appl.* **2003**, *150*, 165–174. [CrossRef]
14. Kim, J.; Oh, W.; Moon, G. A novel two-switch active clamp forward converter for high input voltage applications. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 3028–3034. [CrossRef]
15. Ko, S.; Jeong, Y.; Rorrer, R.; Park, J.-D. High efficiency asymmetric dual active clamp forward converter with phase-shift control of small conduction loss. In Proceedings of the 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 15–19 March 2020; pp. 1866–1871. [CrossRef]
16. Yau, Y.T.; Jiang, W.Z.; Hwu, K.I. Light-load efficiency improvement for flyback converter based on hybrid clamp circuit. In Proceedings of the 2016 IEEE International Conference on Industrial Technology (ICIT), Taipei, Taiwan, 14–17 March 2016; pp. 329–333. [CrossRef]
17. Xue, L.; Zhang, J. Highly efficient secondary-resonant active clamp flyback converter. *IEEE Trans. Ind. Electron* **2018**, *65*, 1235–1243. [CrossRef]
18. Chen, M.; Xu, S.; Huang, L.; Sun, W.; Shi, L. A novel digital control method of primary-side regulated flyback with active clamping technique. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, 1–13. [CrossRef]
19. Das, P.; Laan, B.; Mousavi, S.A.; Moschopoulos, G. A nonisolated bidirectional ZVS-PWM active clamped DC-DC converter. *IEEE Trans. Power Electron.* **2009**, *24*, 553–558. [CrossRef]
20. Wu, X.; Zhang, J.; Ye, X.; Qian, Z. Analysis and design for a new ZVS DC-DC converter with active clamping. *IEEE Trans. Power Electron.* **2006**, *21*, 1572–1579. [CrossRef]
21. Fan, S.; Sun, L.; Duan, J.; Zhang, K. Improved active clamped ZVS buck converter with freewheeling current transfer circuit. *IET Power Electron.* **2019**, *12*, 1341–1348. [CrossRef]
22. Hwu, K.; Tai, Y.; Tu, H. Implementation of a dimmable LED driver with extendable parallel structure and capacitive current sharing. *Appl. Sci.* **2019**, *23*, 5177. [CrossRef]